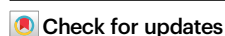


# System-level integration of halide perovskite optoelectronics for its commercial deployment

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Halide perovskites have emerged as a compelling material for a broad range of optoelectronic applications, including light-emitting diodes, phototransistors, light-sensing and imaging systems. To enable practical application and compatibility with existing consumer electronics, they must be integrated with heterogeneous electronic platforms, such as complementary metal-oxide-semiconductor chips or thin-film transistors. Such integration is pivotal for transitioning perovskite technologies from laboratory demonstrations to commercial applications. In this perspective, we summarize recent progress in the system-level integration of perovskite optoelectronics with driving back-planes, compare key performance metrics with industrial benchmarks, discuss major challenges, and outline future directions and application prospects for perovskite optoelectronics.

Metal halide perovskites (MHPs) have emerged as prominent materials for a broad range of optoelectronic devices such as solar cells, light-emitting diodes (LEDs), photodetectors (PDs), etc., owing to their superior optoelectronic properties and low-cost fabrication<sup>1–3</sup>. Their general chemical formula is  $ABX_3$ , where A is a monovalent cation (such as methylammonium, formamidinium, or  $Cs^+$ ), B is a divalent metal cation (typically  $Pb^{2+}$ ), and X represents halide anions ( $Cl^-$ ,  $Br^-$ , or  $I^-$ ), enabling substantial tunability in chemical composition<sup>4,5</sup>. For the crystal structure, MHPs typically adopt a three-dimensional (3D) network of corner-sharing  $BX_6$  octahedra with A-site cations occupying the octahedral cavities. The corner-sharing  $BX_6$  octahedra act as the fundamental structural unit, and geometric distortions within them strongly influence key material properties (Fig. 1a). The valence band maximum primarily originates from the antibonding hybridization between metal *s* and halide *p* orbitals, while the conduction band minimum derives from the antibonding hybridization between metal *p*

and halide *p* orbitals, all of which exhibit relatively weak bonding characters (Fig. 1b)<sup>6–8</sup>. As a result, even slight variations in the  $BX_6$  octahedra, such as changes in the B–X bond length, octahedral tilting, or distortions, can directly alter the electronic structure and the optoelectronic properties of MHPs.

The  $BX_6$  octahedra can assemble into a variety of negatively charged octahedral networks that are stabilized by appropriately selected A-site cations. Variations in A-site cation species have a profound influence on the crystal structure of MHPs, and consequently, on their optoelectronic properties<sup>9,10</sup>. These variations enable MHPs to exhibit diverse structural dimensionalities, including zero-dimensional (0D), one-dimensional (1D), two-dimensional (2D), quasi-2D and 3D configurations, as illustrated in Fig. 1c. For instance, the incorporation of bulky A-site cations often promotes the formation of 2D perovskites with self-assembled quantum-well structures<sup>11–13</sup>. In addition, by precisely controlling the spacings and connectivity within the octahedral

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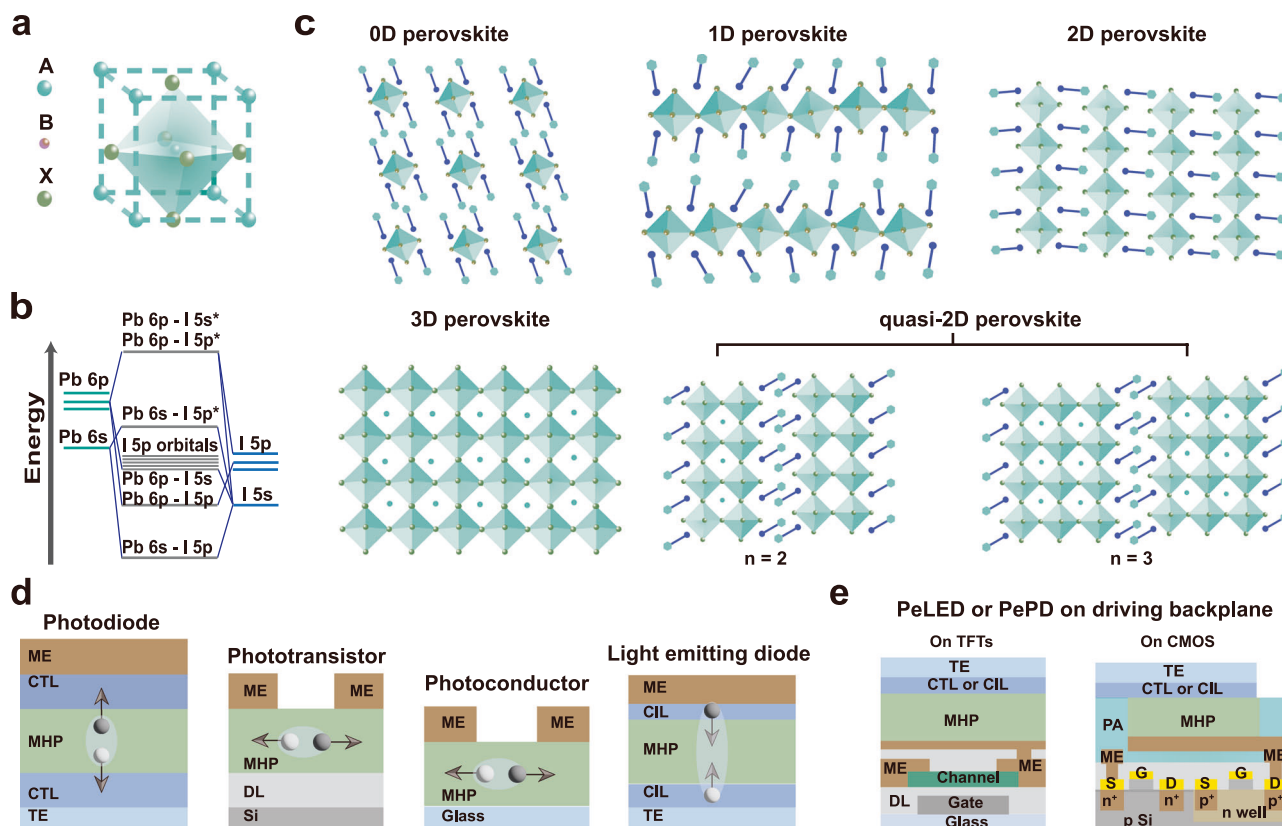


**Fig. 1 | Crystal structures and device architectures.** **a** Unit cell of perovskite crystal with the chemical formula  $ABX_3$ , where A is a monovalent cation, B is a divalent cation, and X is a halide anion. **b** Typical energy band structure of lead iodide perovskites. **c** Representative dimensionalities of perovskites, including zero-dimensional (0D), one-dimensional (1D), two-dimensional (2D), quasi-2D and three-dimensional (3D) structures. **d** Illustration of perovskite optoelectronic device configurations. ME, metal electrode; CTL, charge-transporting layer; MHP,

metal halide perovskites; TE, transparent electrode; DL, dielectric layer; Si, silicon; CIL, charge-injection layer. **e** Typical device structures of perovskite LEDs (PeLEDs) or perovskite PDs (PePDs) integrated with driving backplanes such as thin-film transistors (TFTs) and complementary metal-oxide-semiconductor (CMOS) circuits. PA, passivation layer; S, source; D, drain; p Si, p-type silicon; n well, n-type silicon well; n', heavily doped n-type silicon; p', heavily doped p-type silicon.

network, superlattice structures can be engineered to achieve tailored optical and electronic properties<sup>14–16</sup>. Moreover, long-chain organic A-site cations can drive the formation of MHP quantum dots (QDs) and/or nanowires, offering further opportunities for tuning material functionality and device performance<sup>17–19</sup>. Collectively, these structural variations highlight the remarkable versatility of MHPs and their potential for enabling customizable applications in optoelectronic devices.

The exceptional optoelectronic properties of MHPs have positioned them as a rising star in next-generation optoelectronic technologies. Up to now, MHPs have been widely applied in PDs, phototransistors, photoconductors and LEDs (Fig. 1d), and their device performance has undergone remarkable advancement over the past decade<sup>20–24</sup>. Perovskite PDs (PePDs) already exhibit performance metrics comparable to those of commercial counterparts, while perovskite LEDs (PeLEDs) have achieved high external quantum efficiencies (EQEs) exceeding 28% in the green and red spectral regions and over 20% for blue emission<sup>3,25,26</sup>. Moreover, PeLEDs show narrow emission linewidths that are advantageous for achieving high color purity<sup>3,25,26</sup>. The high color purity and energy-efficient features make PeLEDs promising for micro-display applications, i.e., augmented reality (AR) and virtual reality (VR) near-eye micro-displays. Despite rapidly expanding potential, the commercial translation of PeLEDs ultimately depends on their reliable integration with driving backplanes, such as thin-film transistor (TFT) arrays and complementary metal-oxide-semiconductor (CMOS) chips.

Monolithic heterogeneous integration of electrical driving backplanes with functional optoelectronic devices represents a transformative strategy for advancing the semiconductor industry. Representative architectures for perovskite optoelectronic devices enabled by such heterogeneous integration are illustrated in Fig. 1e. Several studies have reported the successful heterogeneous integration of PeLEDs or PePDs with TFT or CMOS circuits, achieving uniform, high-resolution pixel arrays and fast switching speeds<sup>27</sup>. Besides, diverse deposition and growth techniques for MHPs, such as blade coating, epitaxial growth, and thermal evaporation, have been adopted to enable large-area fabrication and compatibility with driving backplanes, thereby broadening the processing toolkit for perovskite-based heterogeneous integration<sup>28–30</sup>. Despite these advances, achieving robust heterogeneous integration while maintaining excellent optoelectronic device performance remains a sizable challenge. Presently, major obstacles lie in the substantial mismatches in processing conditions and material properties between perovskites and conventional driving backplanes, particularly in terms of interfacial bonding materials, fabrication environments, and material stability. Such incompatibilities generally lead to increased defect densities, reduced charge-transfer efficiency and overall device degradation. These challenges are further compounded by the pronounced sensitivity of perovskites to processing environments, such as polar solvents, oxygen, and temperature fluctuations, which can exacerbate chemical and structural degradation during integration<sup>31,32</sup>. In addition, scalable fabrication techniques capable of ensuring precise alignment

and defect-free interfaces remain underdeveloped, posing additional barriers of large-scale implementation. Overcoming these challenges will be essential for unlocking the full potential of perovskite-based heterogeneous devices in next-generation optoelectronic technologies, including high-resolution displays, on-chip light sources, and advanced imaging.

In this Perspective, we first outline the key requirements for the system-level integration of perovskite optoelectronic devices with driving backplanes. We then summarize recent progress in the heterogeneous integration of PeLEDs and PePDs with established driving backplanes. We also discuss the key challenges that limit practical deployment, including interfacial coupling, materials compatibility, scalability, precising patterning, and electrical and optical matching. Finally, we highlight promising future research directions and advanced applications of perovskite-based heterogeneous integration devices. Particularly, the convergence of perovskite optoelectronics with neuromorphic architectures presents an exciting emerging avenue that could reshape the landscape of next-generation optoelectronic technologies.

### Fundamentals of perovskite heterogeneous integration

Heterogeneous integration is a critical step towards realizing the commercial potential of perovskite optoelectronic devices, including micro-displays, PDs, and on-chip light sources. Uniform patterning, robust interfacial connection and reliable heterogeneous integration technique stand out as critical prerequisites for perovskite heterogeneous integrations.

### Perovskite patterning

Patterned perovskite optoelectronic devices are essential for heterogeneous integration with driving backplanes. Pre-patterned substrate techniques represent one of the most widely explored bottom-up methods for fabricating perovskite arrays (Fig. 2a). By leveraging space-confined growth or hydrophilic-hydrophobic surface contrast, the crystallization of perovskites can be effectively controlled into well-defined patterns. Besides, nanoimprinting is a substrate-independent patterning method that can overcome the substrate limitation associated with heterogeneous integration (Fig. 2a). The solution processability of halide perovskites makes them inherently compatible with imprinting. The liquid or quasi-liquid precursor can be confined by a patterned stamp and solidifies into the replicated structures<sup>33</sup>. At present, nanoimprinting is regarded as the most promising candidate for overcoming the resolution and process limitations of conventional photolithography, with state-of-the-art demonstrations achieving resolutions as high as 25,400 pixels per inch (ppi)<sup>34</sup>.

### Interfacial connection

Interfacial connection plays a pivotal role in heterogeneous integration, serving as the functional bridge that ensures robust mechanical adhesion, efficient charge transport and effective optical coupling between perovskite devices and adjacent electronic components (Fig. 2b). As directly fabricating perovskite devices on driving backplanes, these layers may function as CTLs, passivation layers, charge-quenching layers or multifunctional interlayers. In all cases, they must possess chemical and thermal compatibility with both perovskites and adjacent materials, while supporting the growth of high-quality perovskite films or following functional layers with minimal interfacial defects. When fabricating perovskite devices and driving backplanes separately, the design of connection layers is even more critical, as they must accommodate surface roughness, ensure mechanical conformity and maintain electrical continuity throughout the transfer-printing process. In transfer processes, the adhesion between the perovskite and the connection layer must be stronger than that

between the perovskite and the sacrificial layer to guarantee successful pickup and release.

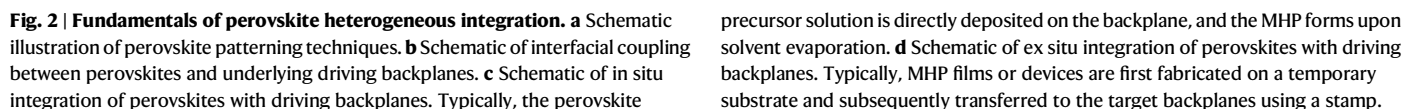
### Heterogeneous integration techniques

Heterogeneous integration techniques can be broadly categorized into *in situ* and *ex situ* strategies. *In situ* heterogeneous integration involves directly fabricating perovskite devices on the target substrate through techniques such as spin-coating, blade-coating or thermal evaporation (Fig. 2c). This *in-situ* approach enables seamless integration of complex devices with minimal interfacial contamination or mechanical damage, and is particularly advantageous for architectures requiring precise alignment of stacked functional units. In contrast, *ex situ* heterogeneous integration fabricates perovskite devices and driving backplanes separately, followed by assembly through methods such as transfer printing, lamination or deterministic pick-and-place processes (Fig. 2d). This method provides greater flexibility in material selection and processing conditions, allowing perovskite devices to be processed under optimal conditions before integration, while also offering promising compatibility with arbitrary substrates, such as curved, textured or otherwise non-planar surfaces.

### Progress and remaining challenges of perovskite heterogeneous integration

**Integrating PeLEDs on driving backplanes.** PeLEDs exhibit high color purity, tunable emission, and can be precisely patterned using thermal evaporation, inkjet printing, *in situ* lithography or nanoimprint lithography, making them ideal candidates for integration with driving backplanes to realize high-resolution full-color displays. Among these approaches, thermal evaporation, widely used in commercial organic LEDs manufacturing, enables the fabrication of uniform, large-area and ultrafine patterned LED pixels through metal masks, offering compatibility with existing TFT manufacturing processes. Importantly, since no organic solvents are involved, the thermally evaporated perovskite films allow the deposition of multi-color PeLED pixels without chemical cross-contamination. Li et al. developed a tri-source co-evaporation strategy incorporating a multifunctional Lewis-base additive to *in situ* form high-quality perovskite nanocrystal films. PeLEDs fabricated by this thermal evaporation route achieved a peak EQE of 16.4% and were successfully integrated onto a 6.67-inch TFT backplane to deliver an active-matrix display with a resolution of 1080 × 2400 (Fig. 3a–c)<sup>35</sup>. By constructing Cs<sub>4</sub>PbBr<sub>6</sub>/CsPbBr<sub>3</sub> core-shell structures, Du et al. reported high-resolution PeLED arrays via vacuum deposition, achieving a record EQE of 8.0% for thermally evaporated PeLEDs and further highlighting their compatibility with active-matrix architectures<sup>36</sup>. Besides, thermally evaporated PeLEDs have also been integrated onto MoS<sub>2</sub> TFT backplanes, demonstrating the universality of this strategy for heterogeneous integration of perovskite optoelectronic devices across diverse substrates<sup>37</sup>. Overall, these results demonstrate the promising compatibility of thermal evaporation deposition techniques with TFT production lines and underscore the early-stage integration feasibility of PeLEDs for integration into high-resolution, large-area, and flexible display panels.

Li et al. developed a nanosurface reconstruction strategy to stabilize CsPbI<sub>3</sub> QDs, enabling PeLEDs with a high EQE of 28.5% and markedly improved operational stability<sup>38</sup>. These PeLEDs were further integrated with customized TFT backplanes to realize active-matrix displays (Fig. 3d), achieving a peak EQE of 23.6% at 300 cd m<sup>-2</sup>, highlighting a key advance in PeQD-based optoelectronics for heterogeneous integration. Building on this progress, the same group reported microsecond-response active-matrix displays by integrating PeLEDs with TFT backplanes using individually passivated perovskite nanocrystals, demonstrating response speeds comparable to those of active-matrix LEDs based on organic dyes and other QDs<sup>27</sup>. Critically, this strategy is compatible with diverse PeQD compositions and various solution-processing techniques, enabling high-refresh-rate full-



feasibility of in situ integrating perovskite materials with TFT backplanes for next-generation, low-dose flat-panel X-ray detectors. Beyond rigid platforms, integrating perovskite PDs with indium gallium zinc oxide (IGZO) TFT panels also enables flexible image sensors. Zou et al. demonstrated a flexible image sensor by integrating PePDs with IGZO TFT panels, providing a low-cost, high-performance alternative to conventional amorphous silicon-based sensors<sup>41</sup>. To enhance the mechanical anchoring between perovskites and TFT substrates, Deumel et al. adopted a photoresist grid as an adhesion promoter for thick MAPbI<sub>3</sub> layers<sup>42</sup>. Using this method, they integrated perovskite films onto a backplane with a 640 × 480-pixel array and a pixel density of 508 ppi, achieving a pixelated X-ray detector sensitivity of 1060  $\mu\text{C Gy}_{\text{air}}^{-1} \text{cm}^{-2}$ . Jin et al. introduced a perovskite X-ray detector architecture incorporating a dark-current-shunting electrode functioning

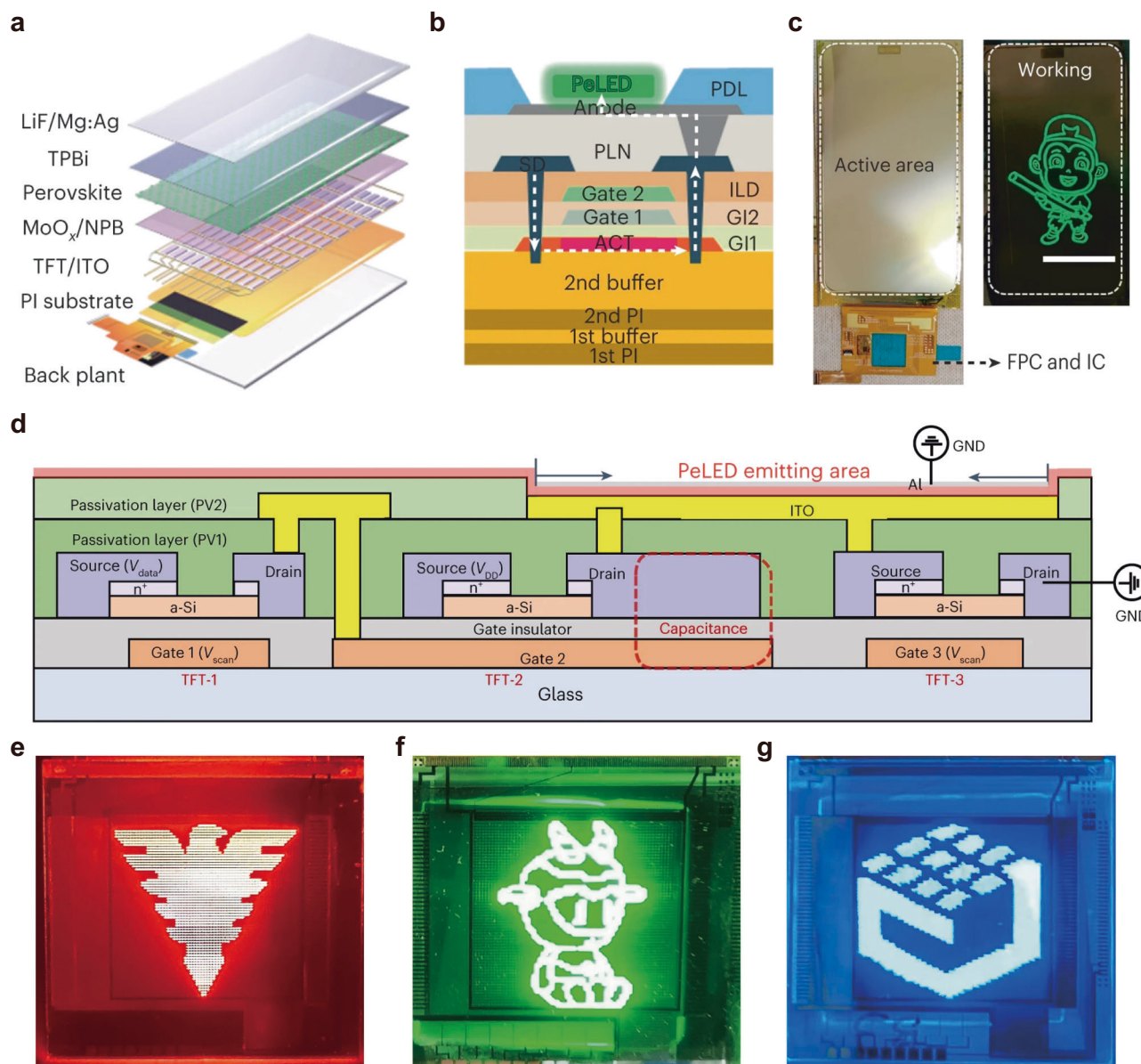


**Fig. 3 | Integrating PeLEDs on driving backplanes.** **a** Structural schematic diagram of the display panel by integrating PeLEDs with TFT backplanes. ITO, indium tin oxide; PI, polyimide; NPB, N,N'-bis-(1-naphthalenyl)-N,N'-bis-phenyl-(1,1'-biphenyl)-4,4'-diamine; TPBi, 1,3,5-tri(N-phenylbenzimidazol-2-yl)benzene. **b** Cross-sectional diagram of the TFT structure beneath each sub-pixel, with arrows indicating the current flow. ACT, activated layer; GI, gate insulation layer; ILD, insulation layer dielectric; PLN, planarization layer; PDL, pixel definition layer. **c** Photograph of the active-matrix PeLED display panel and its operating state. Scale bar, 5 cm. FPC, flexible printed circuit; IC, integrated circuit. **d** Schematic of the TFT backplane structure. The multilayers of PeLEDs uniformly cover the entire TFT

backplane, with the co-cathode connected to grounded (GND). Each pixel integrates three TFTs, address TFT-1, drive TFT-2 and reset TFT-3, combined with a storage capacitor to regulate the PeLED. a-Si, amorphous silicon; n<sup>+</sup>, n-doped region; V<sub>data</sub>, data voltage; V<sub>scan</sub>, scan voltage; V<sub>DD</sub>, supply voltage. The red dashed box denotes the capacitor area. **e–g** Digital photographs of the 1-inch red (**e**), green (**f**) and blue (**g**) active-matrix PeLEDs displaying cartoon images. Panel reproduced with permission from: (**a–c**), ref. 35, Copyright©2023, under exclusive license to Springer Nature Limited. **d**, ref. 38, Copyright©2024, under exclusive license to Springer Nature Limited. **e–g** ref. 27, Copyright©2024, under the terms of the Creative Commons CC BY license.

as a blanking unit to effectively suppress dark current to near-zero levels, and integrated it on a 64 × 64 In<sub>2</sub>O<sub>3</sub> TFT backplane<sup>43</sup>. This strategy establishes a generalizable approach for minimizing dark current and enhancing signal-to-noise ratio, advancing high-precision and low-noise perovskite-based X-ray and PD array technologies. Perovskites can also be directly integrated with CMOS to build high-performance imaging and sensing devices. Yen et al. proposed a CMOS-compatible hybrid image sensor architecture by directly integrating PePDs onto a 0.18 μm CMOS readout circuit, realizing a fully integrated 40 × 40 μm<sup>2</sup> hybrid perovskite-CMOS array<sup>44</sup>. This work

represented the first demonstration of perovskite-CMOS integration under low-bias operation, showcasing the feasibility of monolithic perovskite-CMOS platforms for compact, low-cost and high-sensitivity imaging. Song et al. demonstrated monolithic integration of PePDs with silicon readout integrated circuits, enabling high-resolution 2D and 3D imaging within a unified architecture (Fig. 4a)<sup>45</sup>. The hybrid device enables precise 2D imaging and fast top-electrode-controlled indirect time of flight-based 3D depth sensing (Fig. 4b, c), highlighting the potential of in situ integrating perovskite optoelectronic devices on CMOS-compatible substrates. Liu et al. developed a high-

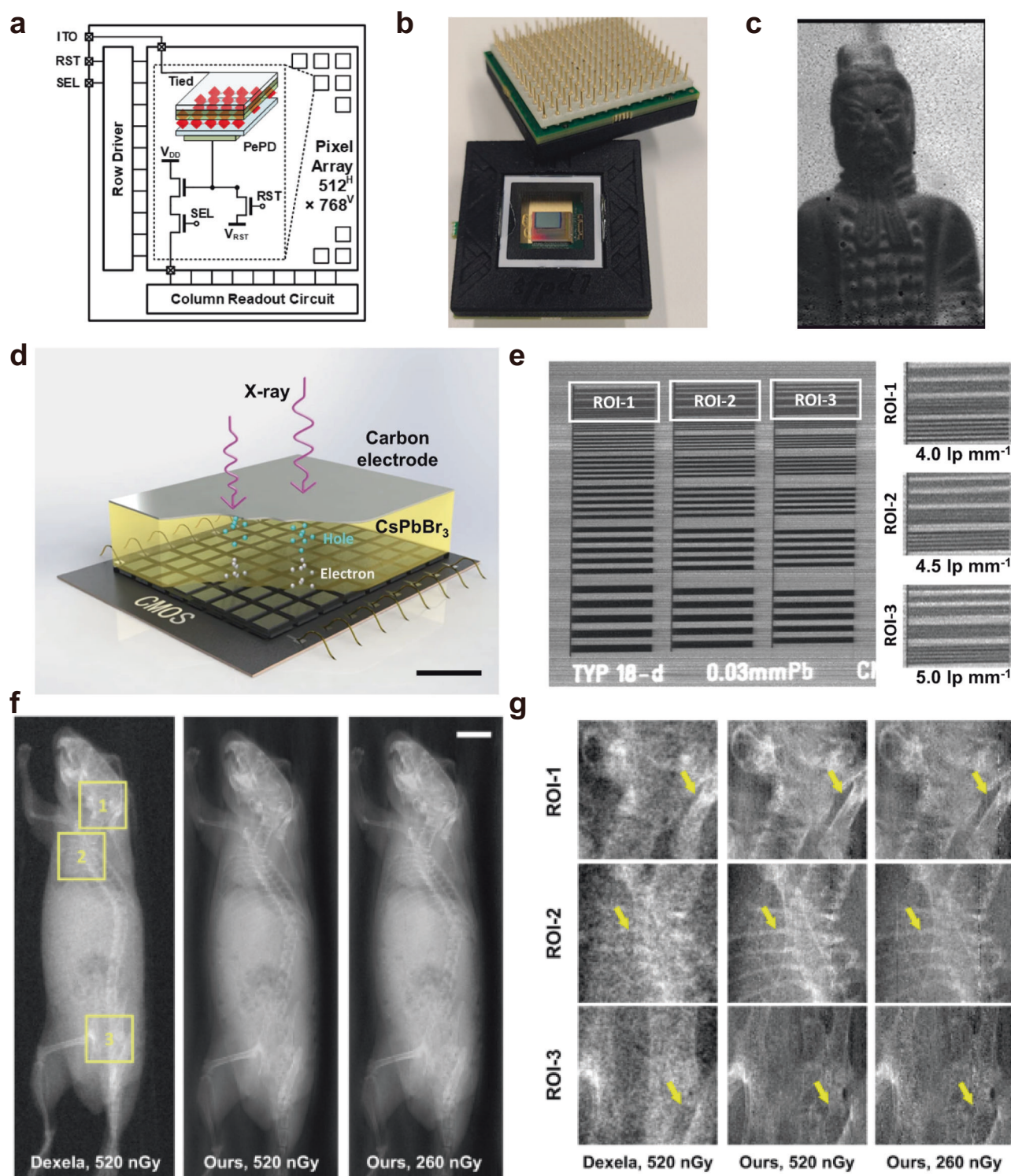


**Fig. 4 | Integrating PePDs on driving backplanes.** **a** Structural schematic of a perovskite image sensor. RST, reset transistor; SEL, select transistor. **b** An optical image of bonded and packed perovskite-based image sensors. **c** Intensity image captured by the prototype perovskite image sensor. **d** Schematic illustration of a perovskite X-ray detector. X-ray photons generate electron-hole pairs within the perovskite film, and the electrons drift toward the CMOS pixels under an applied bias to finally form an X-ray image. Scale bar, 200  $\mu\text{m}$ . **e** X-ray image of a standard resolution test pattern. Three regions of interest (ROIs) are highlighted, and the bars with a spatial resolution of 5.0 lp mm<sup>-1</sup> in ROI-3 are distinctly visible.

**f** Radiographic images of a mouse. The first column shows an image captured using a commercial indirect-conversion CMOS X-ray detector with a pixel size of 74.8  $\mu\text{m}$ . The second and third columns show images obtained from a direct perovskite-CMOS X-ray detector with an 83.2  $\mu\text{m}$  pixel size at two different dose levels: 100% and 50%. Scale bar, 2.0 mm. **g** Magnified ROIs. The skull, ribs, and pelvis captured by the direct perovskite-CMOS X-ray detector appear significantly sharper and less noisy, even at 50% of the radiation dose. Panels reproduced with permission from: **a–c**, ref. 45, Copyright©2024, American Chemical Society. **d–g**, ref. 46, Copyright©2024, under the terms of the Creative Commons CC BY license.

**Table 1 | Representative PeLED performance metrics for display applications in comparison with industrial benchmarks**

| Device performance                                     | Record values               | Benchmarks             |
|--------------------------------------------------------|-----------------------------|------------------------|
| EQE (Green/Red)                                        | > 28% <sup>3,26</sup>       | > 20%                  |
| EQE (Blue)                                             | > 20% <sup>27</sup>         | > 15%                  |
| T <sub>90</sub> lifetime (Device operational lifetime) | > 700 h <sup>96</sup>       | > 10,000 h             |
| Full width at half maximum                             | < 25 nm <sup>35</sup>       | < 30 nm                |
| Pixel density                                          | > 100,000 ppi <sup>53</sup> | > 3000 ppi (for AR/VR) |
| Manufacturing uniformity                               | 98.9% <sup>35</sup>         | > 99.5%                |

**Table 2 | Representative PePD performance metrics in comparison with industrial benchmarks**

| Device performance       | Record values                                                                          | Benchmarks                                                                           |
|--------------------------|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------|
| Responsivity             | > 10 <sup>4</sup> A W <sup>-1</sup> <sup>97</sup>                                      | 0.1 ~ 10 A W <sup>-1</sup>                                                           |
| Specific detectivity     | > 10 <sup>13</sup> Jones <sup>97</sup>                                                 | > 10 <sup>13</sup> Jones                                                             |
| Linear dynamic range     | 191 dB <sup>98</sup>                                                                   | > 120 dB                                                                             |
| Response time            | < 1 μs <sup>98</sup>                                                                   | < 1 ms (for image)                                                                   |
| Stability                | Limited standardized data                                                              | ~1000 h                                                                              |
| Manufacturing uniformity | ~ 98.42% <sup>99</sup>                                                                 | Commercial standards                                                                 |
| X-ray sensitivity        | > 10 <sup>5</sup> μC Gy <sub>air</sub> <sup>-1</sup> cm <sup>-2</sup> <sup>[100]</sup> | 20 μC Gy <sub>air</sub> <sup>-1</sup> cm <sup>-2</sup>                               |
| X-ray detection limit    | < 1 μGy <sub>air</sub> s <sup>-1</sup> <sup>[100]</sup>                                | 5.5 μGy <sub>air</sub> s <sup>-1</sup>                                               |
| X-ray spatial resolution | > 10 lp mm <sup>-1</sup> <sup>[100]</sup>                                              | > 5 lp mm <sup>-1</sup> for radiography and > 10 lp mm <sup>-1</sup> for mammography |

performance direct X-ray detector by screen-printing CsPbBr<sub>3</sub> directly onto CMOS substrates, achieving a spatial resolution exceeding 5.0 lp mm<sup>-1</sup> (Fig. 4d, e)<sup>46</sup>. Moreover, this direct perovskite-CMOS X-ray detector demonstrated better spatial resolution compared with indirect CMOS detectors, while also enabling effective low-dose imaging performance (Fig. 4f, g)<sup>46</sup>. Wang et al. demonstrated heterogeneous monolithic integration of perovskite pixels onto CMOS circuits, presenting a 640 × 512 image sensor chip with a high pixel-fill factor of 98.7%<sup>47</sup>. This was realized by directly spin-coating perovskite precursor solutions onto CMOS, thus preserving the integrity of the underlying circuitry.

**Remaining challenges for heterogeneous integration.** Heterogeneous integration of perovskite optoelectronic devices with driving backplanes has progressed rapidly, yet critical gaps remain between laboratory demonstrations and commercial translation. As summarized in Tables 1 and 2, representative PeLEDs and PePDs have achieved performance metrics approaching or even exceeding industrial benchmarks. Notably, the primary barriers have shifted from intrinsic device performance to reliability and manufacturability. For PeLEDs, although efficiency, brightness, and color purity now rival industrial standards in controlled environments, operational stability under real-world conditions, including thermal cycling, humidity, and continuous electrical bias, remains the defining limitation. In contrast, PePDs already surpass commercial counterparts in key metrics such as responsivity, detectivity, and X-ray sensitivity. In the context of PeLED- and PePD-based heterogeneous integration, future efforts should extend beyond achieving record values in individual metrics and instead focus on the coordinated optimization of system-level performance, integration compatibility and long-term reliability. Key challenges include interfacial coupling and material compatibility, which are critical for mitigating interfacial degradation, ion migration,

and parasitic chemical reactions over time. Additional challenges lie in scalability and high-resolution patterning, as laboratory-scale processes such as spin-coating remain incompatible with high-throughput, large-area production, and uniform device performance across large substrates. Electrical compatibility and optical crosstalk must also be carefully managed to ensure reliable operation with commercial driving backplanes under practical biasing conditions and complex circuit architectures. Addressing these industry-relevant challenges, rather than solely pursuing lab-scale record device metrics, will be essential for translating the intrinsic advantages of perovskites into commercially viable integrated optoelectronic systems.

**Interfacial coupling and materials compatibility.** Despite the remarkable advances in integrating perovskite optoelectronic devices with driving backplanes, interfacial coupling remains one of the most critical challenges that hinders device stability, performance uniformity, and large-scale manufacturability. Perovskites possess the coefficients of thermal expansion on the order of 10<sup>-5</sup>–10<sup>-4</sup> K<sup>-1</sup> and often exhibit pronounced anisotropy<sup>48–50</sup>, while silicon and oxide materials typically exhibit much lower values on the order of 10<sup>-6</sup> K<sup>-1</sup><sup>[51,52]</sup>. This disparity inevitably results in interfacial stress, cracking, and delamination, posing constraints on achieving intimate and damage-free films and representing a primary source of interfacial failure. Meanwhile, mismatches in crystal structure and surface energy between perovskite layers and underlying electronic substrates can induce lattice strain accumulation, rough film morphology, weak interfacial adhesion and interfacial trap states, resulting in non-radiative recombination losses and device instability.

The electronic properties of interfacial connection layers govern energy band alignment and carrier transport kinetics across heterogeneous perovskite-backplane interfaces. Misalignment between the perovskite layer and backplane electrodes leads to charge accumulation and inefficient carrier injection, while halide migration across the interface remains a primary degradation pathway that can induce metal corrosion, dielectric breakdown, and backplane instability. In addition, integration is constrained by CMOS back-end-of-line thermal budgets, which typically limit processing temperatures to below 400 °C to preserve the integrity of underlying metal interconnects.

Addressing these challenges requires interface engineering that extends beyond the reduction of contact resistance. It is essential to mitigate chemical incompatibility while developing scalable strategies to accommodate the mechanical stress arising from structural and thermal mismatches, both of which compromise long-term operational stability. Promising approaches include the incorporation of mechanically compliant or gradient buffer layers to bridge disparities in coefficients of thermal expansion and elastic moduli, thereby suppressing stress concentration and fracture. In addition, surface-energy modulation using self-assembled monolayers (SAMs) can optimize wetting and nucleation while passivating interfacial trap states. The introduction of ultrathin inorganic barrier layers, such as metal oxides or 2D materials, offers an effective route to suppress ion diffusion and parasitic reactions without sacrificing charge-carrier transport.

Although many strategies have been developed, including surface passivation, SAMs, ultrathin atomic buffer layers, and low-temperature or solvent-free integration techniques that enhance electronic coupling while preserving the intrinsic optoelectronic properties of perovskites, most of these approaches remain material- or process-specific and lack general applicability across diverse architectures. Interfacial layers may also inadvertently introduce parasitic resistance or mechanical stress, thereby compromising overall device performance. A limited understanding of interfacial carrier dynamics, strain evolution and crystal distortion under real operating conditions further constrains the rational design of interfaces. Establishing clear structure–property–function relationships among interfacial materials, device physics, and system-level performance, therefore, remains a

critical challenge. Future efforts should combine in situ characterization, multiscale modeling, and artificial intelligence (AI)-assisted materials and process optimization to clarify the coupled electronic, ionic, and mechanical processes at heterogeneous interfaces. Such advances will be essential for developing more universal and robust interfacial engineering strategies for system-level integrated perovskite optoelectronics.

**Scalability and precise patterning.** Achieving uniform wafer-scale patterned perovskite films with consistent thickness and morphology remains challenging. Owing to the intrinsic sensitivity of solution-processed perovskites to local surface wettability and solvent evaporation kinetics, large-area deposition often results in compositional inhomogeneity and pinhole formation, which induce localized electric-field concentration and degrade device performance. In addition, polar aprotic solvents used in the perovskite precursor inks, such as *N,N*-dimethylformamide (DMF) and dimethylsulfoxide (DMSO), can corrode metal interconnects or organic passive layers in CMOS or TFT backplanes, thereby imposing constraints on process compatibility. Although chemical vapor deposition and other solvent-free techniques can improve compatibility with driving backplanes, they often suffer from inferior device performance. Continued efforts in vapor-phase deposition are therefore required to balance crystallization kinetics and film uniformity, enabling industrial-scale heterogeneous integration.

Precise alignment of perovskite pixels with driving backplanes requires high-resolution and low-damage patterning techniques. Utilizing electron beam etching, researchers have confirmed that perovskite device pixel sizes can be reduced down to ~90 nm, corresponding to a record-high pixel density of 127,000 ppi<sup>53</sup>. This resolution lies within the capability of advanced CMOS manufacturing, thereby enabling the integration of halide perovskites with semiconductor technologies. However, most conventional semiconductor etching methods, although capable of generating high-resolution patterns, remain incompatible with the complex topographies of practical electronic backplanes. TFT and CMOS circuits consist of multilayer interconnects, intricate routing networks and heterogeneous materials, typically resulting in non-planar surface morphologies. Such features complicate perovskite pattern transfer and hinder uniform crystallization. Surface roughness and pixel topography fundamentally govern the thermodynamics of heterogeneous integration by influencing precursor wetting, nucleation kinetics and subsequent film crystallization. Non-planar architectures result in non-uniform precursor distribution and localized thickness variations, which in turn trigger stochastic crystallization and defect formation, particularly at step edges and metal interconnects. These topographic constraints further hinder high-resolution pattern transfer and precise pixel alignment, necessitating the development of conformal or planarization-assisted integration strategies. Achieving wafer-scale uniformity, therefore, requires a transition from conventional deposition to topography-tolerant growth approaches that decouple perovskite film quality from the underlying backplane morphology.

To mitigate the detrimental impacts of backplane roughness and structural complexity on film crystallinity, planarization layers, surface-energy modulation, and conformal deposition methods are essential. For high-fidelity pixel definition, localized contact patterning, soft lithography, and self-aligned nanoimprinting have emerged as promising high-resolution and low-damage approaches that preserve the sensitive perovskite lattice. Vapor-phase deposition also offers superior wafer-scale uniformity and improved compatibility with backplanes compared with solution-based processes. A key priority is to establish topography-tolerant and scalable patterning platforms that preserve intrinsic optoelectronic quality across large-area substrates. Achieving this goal will require the convergence of vacuum-

based growth and high-throughput patterning techniques to suppress stochastic defects and enable reliable heterogeneous integration.

**Electrical compatibility and optical crosstalk.** These represent key challenges in the heterogeneous integration of perovskites with TFT and CMOS backplanes. Electrical compatibility remains a critical bottleneck. Perovskite materials intrinsically exhibit ion migration, interfacial polarization and hysteresis, which interfere with precise voltage and current control required for stable circuit operation. Ion accumulation at interfaces substantially deteriorates charge injection and extraction, leading to pronounced hysteresis under electrical or optical excitation. Moreover, ion buildup alters the local electric-field distribution and impedes carrier transport across the heterogeneous interfaces, particularly when perovskite films are directly deposited on TFT or CMOS substrates. When perovskites are monolithically integrated onto TFT or CMOS substrates, multilayer device stacks inevitably introduce parasitic capacitance, which slows charge transport and limits temporal response. The high dielectric constant and ionic polarizability of perovskites further exacerbate capacitive hysteresis and dynamic instability under alternating bias condition<sup>54,55</sup>. In addition, lateral ion migration and charge diffusion within perovskite films can induce crosstalk currents, thereby decreasing spatial resolution and signal fidelity<sup>56,57</sup>. The limited electromagnetic shielding of perovskite layers also allows noise from underlying drive circuits to couple into the top active devices, which degrades the signal-to-noise ratio<sup>58</sup>.

In addition to electrical compatibility, optical crosstalk is another important concern in backplane-integrated architectures, particularly in dense pixel arrays used for imaging and display applications. Optical crosstalk typically originates from lateral photon propagation within the perovskite layer, scattering in adjacent transport layers, and reflections from underlying metal interconnects and dielectric stacks. Such optical leakage degrades spatial resolution, distorts image contrast and reduces detection accuracy in high-density optoelectronic arrays.

Several strategies can be employed to address these challenges. For electrical compatibility, low-capacitance device architectures, together with optimized transport-layer thickness and dielectric design, can minimize resistance-capacitance delay and voltage lag. Compensation driving schemes, shielding structures, and pixel isolation designs can further suppress capacitive coupling and electrical crosstalk. For optical crosstalk, effective approaches include pixel-level optical isolation, optical confinement layers with refractive-index contrast to suppress lateral photon propagation, and optical stack engineering to reduce scattering and parasitic reflections. In addition, microcavity designs, directional outcoupling structures, and patterned absorptive or reflective interlayers can enhance light confinement within individual pixels. The key objective is to establish electrically stable, optically confined, and array-compatible integration strategies that preserve signal fidelity under practical addressing conditions. Achieving this will be essential for translating the intrinsic optoelectronic advantages of perovskites into high-resolution, high-speed, and reliable backplane-integrated systems.

### Enhancing fundamental material design and device integration

In this section, we outline promising research directions that could propel the next major advances in heterogeneous integrated perovskite optoelectronic systems. A particular emphasis is on AI-driven materials discovery, which offers the potential to accelerate the identification, screening and optimization of perovskite compositions and interfacial materials for robust device integration. Meanwhile, bio- and nature-inspired patterning methods for solution-processed perovskite films and QDs are explored as means to achieve precise, scalable, and high-performance device architectures. By addressing the remaining challenges through a synergistic approach combining materials

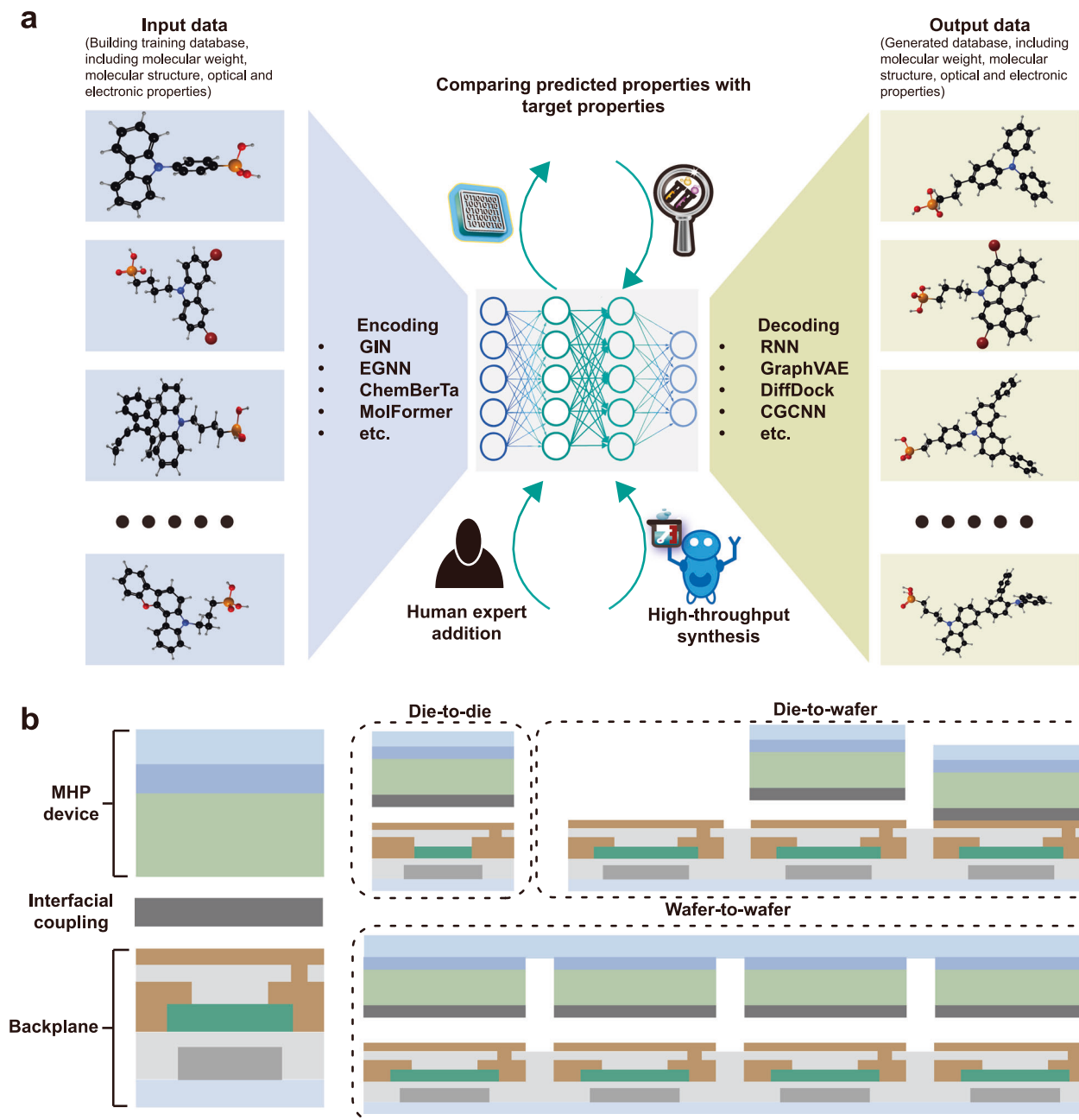


**Fig. 5 | Promising future directions on perovskite heterogeneous integration devices. a** AI-driven materials discovery and screening workflow. GIN, graph isomorphism network; EGNN, equivariant graph neural network; ChemBERTa, chemical bidirectional encoder representations from transformers; MolFormer,

molecular transformer; RNN, recurrent neural network; GraphVAE, graph variational autoencoder; DiffDock, diffusion-based docking; CGCNN, crystal graph convolutional neural network. **b** Strategies for interfacial coupling and bonding, including die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W).

science, device engineering, and AI-driven innovation, future research may enable a new generation of high-performance perovskite optoelectronic devices seamlessly integrated with CMOS and/or TFT backplanes.

**AI-driven materials discovery and screening.** Traditionally, materials discovery and screening have relied on trial-and-error experiments and density functional theory (DFT) calculations, both of which are time-consuming and computationally intensive. These conventional approaches typically require iterative synthesis, characterization and parameter optimization, limiting the efficient exploration of the vast chemical space. Besides, advances in characterization techniques have generated increasingly large and complex datasets, posing challenges

in uncovering the meaningful structure-property relationship. In recent years, AI has begun to revolutionize scientific research and materials innovation (Fig. 5a). AI-driven methods can mine extensive materials datasets, learn structure-property relationships and rapidly predict optimal chemical compositions, electronic structures and crystal configurations. This approach thereby significantly reduces the need for trial-and-error experimentation and offers a transformative approach to discover new materials with higher speed, accuracy, and efficiency. By incorporating scientific knowledge and experiment intuition into AI models through appropriate algorithms, including generative models, reinforcement learning and self-supervised learning, researchers can effectively guide the design of next-generation perovskite and interfacial materials.

AI-driven methods can extract latent knowledge from the literature, enabling researchers to identify promising directions for materials design. This capability is particularly valuable for developing multi-functional materials, where complex chemical, mechanical and electronic requirements must be simultaneously satisfied. Besides, AI-driven methods can involve diverse data types, including X-ray diffraction, Raman spectra, molecular structures, electronic structures, and morphological information, allowing the construction of unified models that correlate structural, optical, and electronic properties, thereby yielding deeper insights into material behavior. For instance, Xie et al. developed a natural language processing (NLP) task called structured information inference to extract the complex device-level information<sup>59</sup>. By fine-tuning GPT-3 on an existing PSC FAIR (Findable, Accessible, Interoperable, Reusable) dataset, they achieved >91% accuracy and expanded the dataset for further analysis. Furthermore, AI methods trained on high-throughput DFT calculations can predict key materials properties, such as bandgap, stability, carrier mobility and defect tolerance. For example, Li et al. combined the data-mining machine learning techniques with the non-equilibrium Green's function method and DFT to rapidly predict the electronic properties of MAPbI<sub>3</sub><sup>60</sup>.

AI also offers a data-driven, property-guided, and highly efficient approach to materials design, leveraging large amounts of unlabeled data. By identifying promising candidates before conducting costly experiments, AI-driven workflows can drastically reduce unnecessary trials, allowing researchers to focus on the most promising materials. Shetty et al. addressed the challenge of extracting chemistry-structure-property relationships from the rapidly expanding materials science literature using NLP<sup>61</sup>. They obtained ~300,000 material property entries from ~130,000 abstracts within 60 h, spanning fields including fuel cells, supercapacitors, and polymer solar cells, thereby revealing valuable insights. A key advantage of an AI-driven method is the capability to perform inverse design, enabling the prediction of materials with specific target properties. For example, Noh et al. presented an inverse materials design framework that computationally generates new solid-state materials by learning a continuous representation of *m* known compounds, producing approximately 20,000 hypothetical materials<sup>62</sup>.

Although AI-driven methods are increasingly being introduced into materials discovery, their application to the heterogeneous integration of perovskites with driving backplanes remains at an early stage. Previous studies have primarily focused on related aspects of system-level heterogeneous integration, such as machine-learning-assisted design of buried interface material materials<sup>63</sup>, Bayesian-optimization for perovskite synthesis and process optimization<sup>64</sup>, and deep-learning-based monitoring of large-area film formation<sup>65</sup>. These efforts demonstrate the potential of data-driven approaches to accelerate the identification of compatible interfacial materials, optimize fabrication windows, and improve process reproducibility. However, the extension of such approaches to full system-level integration of perovskite optoelectronic devices remains limited. In particular, future AI-guided integration should address coupled constraints, including interfacial coupling, scalability and electrical matching with driving backplanes. By enabling efficient information extraction, multi-modal data analysis, high-throughput computation, accurate property prediction, inverse design and cost reduction, AI-driven methods are poised to reshape the development pipeline for heterogeneous integration toward system-level deployment.

**Interfacial coupling and bonding technologies.** Taking advantage of mature experience from advanced thin-film micro-display chips, current heterogeneous integration of halide perovskites mainly refers to the traditional thin-film device protocols<sup>66</sup>, i.e., the layer-by-layer deposition onto driving backplanes. However, unlike commercial organic semiconductors deposited by vacuum evaporation, high-

quality perovskite films are predominantly solution-processed and highly sensitive to underlying substrates. For example, large mismatches in coefficients of thermal expansion between the substrate and perovskite layer can impose undesired strain, compromising film integrity and crystallinity<sup>67,68</sup>. To fully unlock the potential of perovskite-based optoelectronics, one must recognize that there are appreciable differences in transparent conductive oxides and commercial heterogeneous electronic backplanes. The interfacial bonding layers offer a promising approach to address this issue by adjusting surface properties and regulating perovskite crystallization toward ideal growth conditions<sup>69,70</sup>. Achieving this requires a fundamental understanding of perovskite nucleation and growth dynamics on heterogeneous backplanes.

Strategies to heterogeneous integration can learn from advanced display or semiconductor packing technologies, where functional chips are bonded onto driving backplanes with high precision. Taking micro-LED displays as an example, bonding technologies are generally categorized as die-to-die (D2D), die-to-wafer (D2W), and wafer-to-wafer (W2W) (Fig. 5b), with D2W bonding emerging as the most popular options owing to mature equipment, low cost, and high production yield<sup>71–73</sup>. Bonding strategies offer a key advantage for perovskite integration, as devices can be deposited onto desired substrates prior to integration, thereby avoiding substrate-dependent crystallization variations. However, isolated dies are incompatible with thin-film perovskite devices, making W2W bonding the most rational strategy for heterogeneous integration. Within W2W bonding, both point-to-point and global bonding approaches are feasible. Point-to-point bonding requires high alignment accuracy, especially high-density integration, while global bonding is easier but typically needs post-etching that may damage fragile perovskite layers. Furthermore, bonding materials and process temperatures must be strictly optimized to prevent device degradation. Thermal-compression and laser-assisted bonding expose perovskite layers to high temperatures, while plasma-activated bonding can degrade the surface. In contrast, eutectic bonding, which employs a low-melting-point alloy to achieve bonding below 150 °C, emerges as a promising strategy for perovskite heterogeneous integration. Nevertheless, both bonding and conventional thin-film integration techniques remain at an early stage, and their limited maturity continues to constrain the development of perovskite-based on-chip optoelectronics, highlighting a critical area for future research.

Full-color PeLED integration on driving backplanes presents a stringent multidimensional challenge. Beyond reliable coupling to the backplane, it requires the simultaneous realization of high-performance red, green, and blue subpixels, precise pixel definition, and process compatibility among distinct emissive materials. Sequential integration is particularly challenging, as the sensitivity of perovskites to solvent exposure and cross-contamination often leads to performance degradation. In addition, mismatches in operating voltage and stability, especially for blue emitters, further complicate circuit-level integration. Achieving full-color micro-displays, therefore, requires the co-optimization of materials selection, subpixel isolation, and driving circuitry. Promising strategies include orthogonal-solvent processing, transfer printing of monochromatic subpixels, and color-conversion schemes. However, both bonding-based and thin-film integration strategies remain at an early stage of development. Progress toward commercially viable systems will depend on the convergence of stable blue emitters, scalable high-resolution patterning, and low-damage heterogeneous integration strategies that bridge materials engineering with display-oriented circuit design.

**Nature-inspired solution patterning approaches.** Nature-inspired patterning leverages evolved biological principles, such as hierarchical self-assembly and programmable surface wettability, to overcome the stochastic limitations of conventional top-down fabrication. By

mimicking natural architectures, these strategies extend beyond structural replication to introduce intrinsic functionalities, including omnidirectional light extraction and enhanced environmental stability, without compromising the optoelectronic properties of the material. For instance, replicating the hierarchical multilayer structures found in iridescent fish scales can reduce internal reflection and enhance light outcoupling, while simultaneously providing a biomimetic barrier against moisture ingress<sup>74</sup>. Strategies such as programmed coffee-ring effect, peptide-mediated self-assembly, and biomineralization-inspired growth have demonstrated the ability to regulate perovskite nucleation kinetics with sub-micron precision. These bio-inspired strategies therefore provide a robust and low-damage route to achieving high-fidelity pixel arrays and long-term operational stability, which are essential for next-generation micro-displays.

Patterned surface wettability, inspired by the lotus leaf effect, is one of the most popular techniques for fabricating patterned optoelectronic devices. By creating hydrophilic-hydrophobic regions, the selective deposition of functional materials can be guided. The contrast in surface energy between hydrophilic and hydrophobic domains is critical for patterning accuracy, as solution-processed perovskites are highly sensitive to local wettability. Patterned substrates with controlled wettability and template geometries can induce directional forces that guide nanocrystal positioning during growth, potentially achieving resolutions beyond the conventional lithographic limits<sup>75</sup>. Diverse approaches to create such patterned wettability include UV Ozone exposure and oxygen plasma treatment, which generate oxygen-rich surface layers to enhance hydrophilicity. These strategies have been successfully applied to fabricate patterned perovskite optoelectronic devices<sup>76,77</sup>. Besides, chemical functional materials, including poly(methyl methacrylate) (PMMA), poly(N,N'-bis(4-butylphenyl)-N,N'-bisphenyl)benzidine (Poly-TPD) and SAMs, have also been adopted to achieve high-contrast wettability patterns<sup>78,79</sup>.

The coffee-ring effect provides another bio-inspired patterning method. During solvent evaporation, non-volatile solutes in a droplet migrate toward the pinned contact line, forming a characteristic ring-shaped pattern. While this effect is typically undesired due to non-uniformity, it can be harnessed to deposit materials selectively when carefully controlled. For example, Li et al. confined solution droplets within pre-patterned hydrophilic regions, enabling nanoparticles to self-assemble into well-defined circuits through the coffee-ring effect, yielding large-area patterns with diverse geometries within one minute while preserving nanoparticle properties<sup>80</sup>. Thus, such strategies can similarly be applied to perovskite films for high-precision patterning.

In general, nature-inspired solution patterning approaches have demonstrated considerable promise for scalable high-precision perovskite device fabrication. Despite remaining challenges such as limited patterning resolution, scalable uniformity, material stability and integration with conventional semiconductor processing, the initial results suggest a highly promising route for future heterogeneous integration of perovskite optoelectronic devices.

## Outlook on perovskite-based optoelectronic applications

**Perovskite integration for AR/VR.** Heterogeneous integration is emerging as a cornerstone for deploying PeLEDs in next-generation AR/VR near-eye micro-displays. The monolithic integration of PeLEDs with waveguides, sensory arrays, and logic units is expected to enable ultra-compact, high-performance systems with unprecedented pixel density and hardware-level intelligence. By bridging emissive materials with advanced CMOS backplanes, such integrated platforms can overcome current limitations in brightness and efficiency, and accelerate the transition from standalone displays to immersive spatial computing environments. In AR applications, LEDs operate under high-intensity ambient light and therefore require high luminance to ensure virtual imagery remains visible against real-world backgrounds.

In VR systems, both brightness and spatial uniformity are essential for an immersive experience, as non-uniformity or luminance imbalance can lead to visual artifacts, discomfort, and a reduced sense of presence. Although PeLEDs have achieved EQEs exceeding 20%, a large fraction of emitted photons remains trapped within the device stack and is dissipated through various lossy channels due to the inefficient light outcoupling<sup>81,82</sup>. This limitation arises in part from the predominantly isotropic orientation of emissive dipoles in polycrystalline PeLEDs<sup>83</sup>, whereas low-dimensional perovskites provide potential routes to induce preferential dipole orientation<sup>82,84</sup>. Moreover, the high refractive indices of perovskites relative to commonly employed charge-injection materials<sup>85</sup>, combined with the large refractive index contrast between the substrate and the air, confines photons in waveguide modes and further limits light extraction. Effective light management strategies are therefore imperative to enhance light outcoupling and improve the feasibility of PeLEDs for AR/VR applications.

Light management strategies can be broadly categorized into extrinsic and intrinsic outcoupling techniques (Fig. 6a). Extrinsic strategies enhance photon extraction by introducing textured structures or optical microcavities that scatter or diffract light beyond the critical angles. For example, Lee et al. reported tandem hybrid OLED-PeLED devices achieving a green EQE of 37% with a narrow spectral width of 27.3 nm<sup>86</sup>, attributed to enhanced light extraction via optical microcavities. The intrinsic outcoupling strategies, focusing on engineering the orientation of transition dipole moments, reducing the effective refractive index, and enhancing photon recycling. For instance, Sun et al. utilized an anisotropic low-index electron-injection layer, 9,10-bis(4-(2-phenyl-1Hbenzo[d]imidazole-1-yl))phenyl anthracene (BPBiPA), in green PeLEDs, producing preferably in-plane transition dipole moments orientation<sup>87,88</sup>. This design yielded EQEs exceeding 30% because of the enhanced light outcoupling efficiency.

Light management in AR/VR systems presents challenges that extend well beyond those encountered in individual LED devices, as emission must be co-optimized with complex downstream optical components. In practical architectures, substantial losses from waveguides, beam splitters, and polarizers prevent high EQEs from translating into the system-level brightness required for operation. Furthermore, conventional outcoupling strategies developed for large-area devices are often incompatible with micro-displays, where pixel miniaturization, angular emission control, and suppression of optical crosstalk are critical. Light management for AR/VR-integrated PeLEDs must therefore move beyond simple light extraction and instead focus on controlled emission directionality and compatibility with compact optical systems. Realizing high-performance micro-displays will require the co-design of emissive materials, outcoupling structures, and holistic optical architectures.

**Perovskite integration with neuromorphic devices.** Artificial neuromorphic devices, inspired by the architecture and function of the biological brain, emulate synaptic plasticity and neuronal behavior in hardware systems (Fig. 6b). Unlike conventional von Neuman architectures, which separate memory and computation units, neuromorphic systems integrate sensing, storage, and processing within a unified framework, thereby enabling low-power and highly efficient data handling. Such architectures are particularly advantageous for emerging AI applications. The excellent intrinsic properties of perovskites, such as high absorption coefficients, tunable bandgaps and long carrier diffusion lengths, make them promising candidates for constructing neuromorphic synapses that directly couple optical stimuli with electronic responses. Since 2016, when Xu et al. demonstrated an artificial synapse based on MAPbBr<sub>3</sub>, perovskite-based synaptic devices have attracted increasing attention<sup>89–91</sup>. The key mechanism that enables perovskites to mimic synaptic functionalities

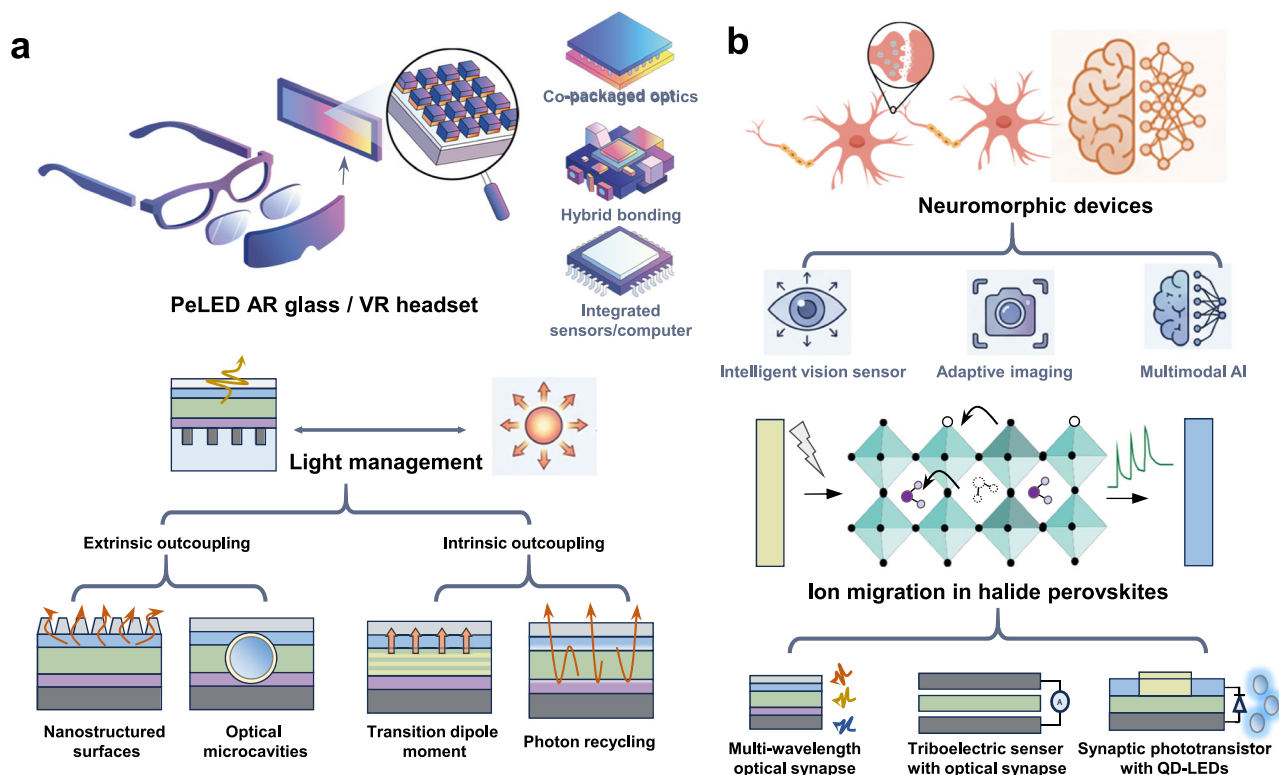


**Fig. 6 | Promising applications of perovskite-based heterogeneous integration devices.** **a** Light management and integration strategies for PeLED-based AR and VR systems. **b** Ion migration in halide perovskites and their integration in neuromorphic computing applications.

is ion migration. Under electrical or optical stimulation, halide ions redistribute within the perovskite lattice, modulating device conductance in a manner analogous to synaptic weight adaptation in biological synapses<sup>92,93</sup>.

Neuromorphic behavior in perovskite-based devices is primarily governed by ion migration, but also arises from the interplay of trap-assisted charge storage and interfacial electrochemical processes. While these mechanisms enable essential synaptic functions such as conductance plasticity, temporal integration, and history-dependent responses, they simultaneously introduce instability. Uncontrolled ion migration accelerates material degradation, promotes trap formation, and induces fluctuations in operating voltage and current. This inherent duality indicates that the same physical processes responsible for neuromorphic functionality can compromise device durability and signal reliability. Achieving reproducible and energy-efficient operation, therefore, requires a transition from empirical material optimization to precise regulation of these dynamic processes. This challenge is particularly critical for backplane-integrated systems, where array-level uniformity and long-term operational stability are as important as the synaptic functionalities themselves.

Beyond adopting perovskites as active materials, integrating perovskites with neuromorphic architectures represents a transformative route for next-generation optoelectronics. Such integration enables near-sensor computing and memory, where perception occurs in perovskite devices while memory and processing are realized in neuromorphic circuits. For example, Seung et al. reported an integrated system combining synaptic phototransistors with QD LEDs, enabling on-device preprocessing that filters noise and amplifies signal contrast via threshold-driven illumination<sup>94</sup>. Similarly, Shan et al. developed a sensory-memory processing platform using a triboelectric nanogenerator as the sensory receptor and QD LEDs as an artificial synapse, demonstrating multi-wavelength synapse-like optical outputs and efficient multimodal information recognition<sup>95</sup>. Such integrated perovskite-neuromorphic devices offer significant potential

for intelligent vision sensors, self-adaptive imaging arrays, and multimodal AI systems. Therefore, we anticipate that perovskite-neuromorphic integration is poised to enable next-generation adaptive optoelectronic interfaces and advanced human-machine communication technologies.

## References

- Li, S. et al. Coherent growth of high-Miller-index facets enhances perovskite solar cells. *Nature* **635**, 874–881 (2024).
- Chen, P. et al. Multifunctional ytterbium oxide buffer for perovskite solar cells. *Nature* **625**, 516–522 (2024).
- Kim, J. S. et al. Ultra-bright, efficient and stable perovskite light-emitting diodes. *Nature* **611**, 688–694 (2022).
- Yang, W., Jo, S.-H. & Lee, T.-W. Perovskite colloidal nanocrystal solar cells: current advances, challenges, and future perspectives. *Adv. Mater.* **36**, 2401788 (2024).
- Chen, P. et al. The promise and challenges of inverted perovskite solar cells. *Chem. Rev.* **124**, 10623–10700 (2024).
- Meloni, S., Palermo, G., Ashari-Astani, N., Grätzel, M. & Rothlisberger, U. Valence and conduction band tuning in halide perovskites for solar cell applications. *J. Mater. Chem. A* **4**, 15997–16002 (2016).
- Sabino, F. P., Zhao, X. G., Dalpian, G. M. & Zunger, A. Impact of symmetry breaking and spin-orbit coupling on the band gap of halide perovskites. *Phys. Rev. B* **110**, 035160 (2024).
- Lu, C.-H., Biesold-McGee, G. V., Liu, Y., Kang, Z. & Lin, Z. Doping and ion substitution in colloidal metal halide perovskite nanocrystals. *Chem. Soc. Rev.* **49**, 4953–5007 (2020).
- Liu, Y. et al. Structurally dimensional engineering in perovskite photovoltaics. *Adv. Energy Mater.* **13**, 2300188 (2023).
- Azmi, R., Utomo, D. S., Liu, Y., Zhumagali, S. & De Wolf, S. Dimensionality engineering of perovskites for stable heterojunction-based photovoltaics. *Nat. Rev. Mater.* **11**, 136–155 (2026).

11. Leung, T. L. et al. Stability of 2D and quasi-2D perovskite materials and devices. *Commun. Mater.* **3**, 63 (2022).
12. Chen, Y. et al. 2D Ruddlesden–popper perovskites for optoelectronics. *Adv. Mater.* **30**, 1703487 (2018).
13. Zhang, L. et al. High-performance quasi-2D perovskite light-emitting diodes: from materials to devices. *Light Sci. Appl.* **10**, 61 (2021).
14. Lei, Y. et al. Perovskite superlattices with efficient carrier dynamics. *Nature* **608**, 317–323 (2022).
15. Cherniukh, I. et al. Perovskite-type superlattices from lead halide perovskite nanocubes. *Nature* **593**, 535–542 (2021).
16. Liu, Z. et al. Metal–halide perovskite nanocrystal superlattice: self-assembly and optical fingerprints. *Adv. Mater.* **35**, 2209279 (2023).
17. Yang, W. et al. Overcoming charge confinement in perovskite nanocrystal solar cells. *Adv. Mater.* **35**, 2304533 (2023).
18. Jang, K. Y. et al. Efficient deep-blue light-emitting diodes through decoupling of colloidal perovskite quantum dots. *Adv. Mater.* **36**, 2404856 (2024).
19. Shao, W. et al. Molecular templating of layered halide perovskite nanowires. *Science* **384**, 1000–1006 (2024).
20. Wang, S. et al. Morphological engineering for high-performance perovskite field-effect transistors. *FlexMat* **2**, 82–106 (2025).
21. Cheng, X. et al. Principles, fabrication, and applications of halide perovskites-based memristors. *FlexMat* **1**, 127–149 (2024).
22. Zhu, Y. et al. Bilayer metal halide perovskite for efficient and stable solar cells and modules. *Mater. Futur.* **1**, 042102 (2022).
23. Zhang, Q. et al. Nanosecond response perovskite quantum dot light-emitting diodes with ultra-high resolution for active display application. *Light Sci. Appl.* **14**, 285 (2025).
24. Hu, C. et al. Recent progress in the patterning of perovskite films for photodetector applications. *Light Sci. Appl.* **14**, 355 (2025).
25. Kim, J. S. et al. Kinetically-controlled intermediate-direct-pinning for homogeneous energy landscapes in quasi-two-dimensional perovskites for efficient and narrow blue emission. *Nat. Commun.* **16**, 9590 (2025).
26. Kong, L. et al. Fabrication of red-emitting perovskite LEDs by stabilizing their octahedral structure. *Nature* **631**, 73–79 (2024).
27. Gao, Y. et al. Microsecond-response perovskite light-emitting diodes for active-matrix displays. *Nat. Electron.* **7**, 487–496 (2024).
28. Meng, Y. et al. Epitaxial growth of  $\alpha$ -FAPbI<sub>3</sub> at a well-matched heterointerface for efficient perovskite solar cells and solar modules. *Adv. Mater.* **36**, 2309208 (2024).
29. Reo, Y. et al. Vapour-deposited high-performance tin perovskite transistors. *Nat. Electron.* **8**, 403–410 (2025).
30. Du, P. et al. Thermal evaporation for halide perovskite optoelectronics: fundamentals, progress, and outlook. *Adv. Opt. Mater.* **10**, 2101770 (2022).
31. Zhu, H. et al. Long-term operating stability in perovskite photovoltaics. *Nat. Rev. Mater.* **8**, 569–586 (2023).
32. Chowdhury, T. A. et al. Stability of perovskite solar cells: issues and prospects. *RSC Adv.* **13**, 1787–1810 (2023).
33. Pourdavoud, N. et al. Photonic nanostructures patterned by thermal nanoimprint directly into organo-metal halide perovskites. *Adv. Mater.* **29**, 1605003 (2017).
34. Lin, L. et al. Nanoscale transfer-printed full-colour ultrahigh-resolution quantum dot LEDs. *Nature* **652**, 349–358 (2026).
35. Li, J. et al. Efficient all-thermally evaporated perovskite light-emitting diodes for active-matrix displays. *Nat. Photon.* **17**, 435–441 (2023).
36. Du, P. et al. Efficient and large-area all vacuum-deposited perovskite light-emitting diodes via spatial confinement. *Nat. Commun.* **12**, 4751 (2021).
37. Ji, S. et al. Perovskite light-emitting diode display based on MoS<sub>2</sub> backplane thin-film transistors. *Adv. Mater.* **36**, 2309531 (2024).
38. Li, H. et al. Nanosurface-reconstructed perovskite for highly efficient and stable active-matrix light-emitting diode display. *Nat. Nanotechnol.* **19**, 638–645 (2024).
39. Zhang, L. et al. Manipulation of charge dynamics for efficient and bright blue perovskite light-emitting diodes with chiral ligands. *Adv. Mater.* **35**, 2302059 (2023).
40. Li, L. et al. Monolithic integration of perovskite heterojunction on TFT backplanes through vapor deposition for sensitive and stable x-ray imaging. *Sci. Adv.* **10**, ead8659 (2024).
41. Zou, T. et al. First demonstration of waferscale heterogeneous integration of Ga<sub>2</sub>O<sub>3</sub> MOSFETs on SiC and Si substrates by ion-cutting process. In *Proceedings of the 2019 IEEE International Electron Devices Meeting* (2019).
42. Deumel, S. et al. High-sensitivity high-resolution X-ray imaging with soft-sintered metal halide perovskites. *Nat. Electron.* **4**, 681–688 (2021).
43. Jin, P. et al. Realizing nearly-zero dark current and ultrahigh signal-to-noise ratio perovskite X-ray detector and image array by dark-current-shunting strategy. *Nat. Commun.* **14**, 626 (2023).
44. Yen, P. W. et al. A hybrid CMOS-imager with perovskites as photoactive layer. In *2016 IEEE SENSORS*. 1–3 (Orlando, FL, USA, 2016).
45. Song, W. et al. Halide perovskite photodiode integrated CMOS imager. *ACS Nano* **18**, 35520–35532 (2024).
46. Liu, Y. et al. Dynamic X-ray imaging with screen-printed perovskite CMOS array. *Nat. Commun.* **15**, 1588 (2024).
47. Wang, X. et al. A monolithically integrated 640 × 512 CMOS-perovskite image sensor, 2024 IEEE European Solid-State Electronics Research Conference (ESSERC), Bruges, Belgium, 213–216 (2024).
48. Jacobsson, T. J., Schwan, L. J., Ottosson, M., Hagfeldt, A. & Edvinsson, T. Determination of thermal expansion coefficients and locating the temperature-induced phase transition in methylammonium lead perovskites using X-ray diffraction. *Inorg. Chem.* **54**, 10678–106851 (2015).
49. Yang, W., Zhong, D., Shi, M., Qu, S. & Chen, H. Toward highly thermal stable perovskite solar cells by rational design of interfacial layer. *iScience* **22**, 534–543 (2019).
50. Ge, C. et al. Ultralow thermal conductivity and ultrahigh thermal expansion of single-crystal organic–inorganic hybrid perovskite CH<sub>3</sub>NH<sub>3</sub>PbX<sub>3</sub> (X = Cl, Br, I). *J. Phys. Chem. C* **122**, 15973–15978 (2018).
51. Tien, C.-L. & Lin, T.-W. Out-of-plane thermal expansion coefficient and biaxial young's modulus of sputtered ITO thin films. *Coatings* **11**, 153 (2021).
52. Yamamoto, N., Makino, H. & Yamamoto, T. Young's modulus and coefficient of linear thermal expansion of ZnO conductive and transparent ultra-thin films. *Adv. Mater. Sci. Eng.* (2011).
53. Lian, Y. et al. Downscaling micro- and nano-perovskite LEDs. *Nature* **640**, 62–68 (2025).
54. Hong, M. J. et al. Time-resolved changes in dielectric constant of metal halide perovskites under illumination. *J. Am. Chem. Soc.* **142**, 19799–19803 (2020).
55. Sahoo, A., Paul, T., Maiti, S. & Banerjee, R. Temperature-dependent dielectric properties of CsPb<sub>2</sub>Br<sub>5</sub>: A 2D inorganic halide perovskite. *Nanotechnology* **33**, 195703 (2022).
56. Cho, C. et al. Efficient vertical charge transport in polycrystalline halide perovskites revealed by four-dimensional tracking of charge carriers. *Nat. Mater.* **21**, 1388–1395 (2022).
57. Jacobs, D. A. et al. Lateral ion migration accelerates degradation in halide perovskite devices. *Energy Environ. Sci.* **15**, 5324–5339 (2022).
58. Zhang, Z. et al. Inorganic halide perovskite electromagnetic wave absorption system with ultra-wide absorption bandwidth and high thermal-stability. *Adv. Electron. Mater.* **9**, 2201179 (2023).

59. Xie, T. Large language models as master key: unlocking the secrets of materials science with GPT. Preprint at <https://doi.org/10.48550/arXiv.2304.02213> (2023).
60. Li, L. et al. Electronic transport of organic-inorganic hybrid perovskites from first-principles and machine learning. *Appl. Phys. Lett.* **114**, 8 (2019).
61. Shetty, P. et al. A general-purpose material property data extraction pipeline from large polymer corpora using natural language processing. *Npj Comput. Mater.* **9**, 52 (2023).
62. Noh, J. et al. Inverse design of solid-state materials via a continuous representation. *Matter* **1**, 1370–1384 (2019).
63. Zhang, C. et al. Machine learning-driven interface material design for high-performance perovskite solar cells with scalability and band-gap universality. *Joule* **10**, 2 (2026).
64. Choe, H., Yoon, H., Kim, I. & Kim, S. Y. Machine learning unlocks new directions in halide perovskite research. *ChemElectroChem* **13**, e202500282 (2026).
65. Laufer, F., Götz, M. & Paetzold, U. W. Deep learning for augmented process monitoring of scalable perovskite thin-film fabrication. *Energy Environ. Sci.* **18**, 1767–1782 (2025).
66. Nathan, A., Chaji, G. R. & Ashtiani, S. J. Driving schemes for a-Si and LTPS AMOLED displays. *J. Disp. Technol.* **1**, 267–277 (2005).
67. Xue, D.-J. et al. Regulating strain in perovskite thin films through charge-transport layers. *Nat. Commun.* **11**, 1514 (2020).
68. Zhao, J. et al. Strained hybrid perovskite thin films and their impact on the intrinsic stability of perovskite solar cells. *Sci. Adv.* **3**, eaao5616 (2017).
69. Sun, C. et al. Multidentate fullerenes enable tunable and robust interfacial bonding for efficient tin-based perovskite solar cells. *Adv. Mater.* **36**, 2410248 (2024).
70. Hui, J. et al. Super strong bonding at the interface between ETL and perovskite for robust flexible optoelectronic devices. *Angew. Chem. Int. Ed.* **64**, e202424483 (2025).
71. Sahoo, K., Harish, V., Ren, H. & Iyer, S. S. A review of die-to-die, die-to-substrate and die-to-wafer heterogeneous integration. *IEEE Electron Dev. Rev.* **2**, 6–31 (2025).
72. Lee, C. Y. et al. 3D integrated process and hybrid bonding of high bandwidth memory (HBM). *Electron. Mater. Lett.* **21**, 395–419 (2025).
73. Gao, G. et al. Scaling package interconnects below 20  $\mu\text{m}$  pitch with hybrid bonding. *2018 IEEE 68th Electronic Components and Technology Conference (ECTC)* 314–322 (San Diego, CA, USA, 2018).
74. Chiu, C.-H., Chien, C.-H., Chien, W.-C. & Chen, Y.-H. To Enhance light lumination of OLED lighting by film included fish scales. *Dig. Tech. Pap.* **47**, 1549–1551 (2016).
75. Jastrzebska-Perfect, P. et al. On-site growth of perovskite nanocrystal arrays for integrated nanodevices. *Nat. Commun.* **14**, 3883 (2023).
76. Piferi, C. et al. Hydrophilicity and hydrophobicity control of plasma-treated surfaces via fractal parameters. *Adv. Mater. Interfaces* **8**, 2100724 (2021).
77. Wu, W. et al. Flexible photodetector arrays based on patterned  $\text{CH}_3\text{NH}_3\text{PbI}_{3-x}\text{Cl}_x$  perovskite film for real-time photosensing and imaging. *Adv. Mater.* **31**, 1805913 (2019).
78. Wu, J. et al. Pinhole-free hybrid perovskite film with arbitrarily-shaped micro-patterns for functional optoelectronic devices. *Nano Lett.* **17**, 3563–3569 (2017).
79. Wang, K. et al. Wettability-guided screen printing of perovskite microlaser arrays for current-driven displays. *Adv. Mater.* **32**, 2001999 (2020).
80. Li, Y. et al. Rapid assembly of large scale transparent circuit arrays using PDMS nanofilm shaped coffee ring. *Adv. Funct. Mater.* **27**, 1606045 (2017).
81. Xu, W. et al. Rational molecular passivation for high-performance perovskite light-emitting diodes. *Nat. Photon.* **13**, 418–424 (2019).
82. Lin, K. et al. Perovskite light-emitting diodes with external quantum efficiency exceeding 20 per cent. *Nature* **562**, 245–248 (2018).
83. Zhao, B. et al. Light management for perovskite light-emitting diodes. *Nat. Nanotechnol.* **18**, 981–992 (2023).
84. Jurow, M. J. et al. Manipulating the transition dipole moment of  $\text{CsPbBr}_3$  perovskite nanocrystals for superior optical properties. *Nano Lett.* **19**, 2489–2496 (2019).
85. Zhao, B. et al. High-efficiency perovskite–polymer bulk heterostructure light-emitting diodes. *Nat. Photon.* **12**, 783–789 (2018).
86. Lee, H.-D. et al. Valley-centre tandem perovskite light-emitting diodes. *Nat. Nanotechnol.* **19**, 624–631 (2024).
87. Sun, S.-Q. et al. Enhancing light outcoupling efficiency via anisotropic low refractive index electron transporting materials for efficient perovskite light-emitting diodes. *Adv. Mater.* **36**, 2400421 (2024).
88. Marcato, T., Kumar, S. & Shih, C.-J. Strategies for controlling emission anisotropy in lead halide perovskite emitters for LED outcoupling enhancement. *Adv. Mater.* **37**, 2413622 (2025).
89. Xu, W. et al. Organometal halide perovskite artificial synapses. *Adv. Mater.* **28**, 5916–5922 (2016).
90. Wang, R. et al. Evaporated copper-based perovskite dynamic memristors for reservoir computing systems. *Adv. Mater. Technol.* **10**, 2400838 (2025).
91. Shao, H. et al. A reconfigurable optoelectronic synaptic transistor with stable  $\text{Zr-CsPbI}_3$  nanocrystals for visuomorphic computing. *Adv. Mater.* **35**, 2208497 (2023).
92. Liu, S. et al. Ionic behaviors of perovskite devices and their neuromorphic applications. *Adv. Funct. Mater.* **36**, e10934 (2025).
93. Niu, W. et al. Incorporating MXene in perovskite for modulating ion migration and enhancing object detection. *Adv. Funct. Mater.* **35**, 2501877 (2025).
94. Seung, H. et al. Integration of synaptic phototransistors and quantum dot light-emitting diodes for visualization and recognition of UV patterns. *Sci. Adv.* **8**, eabq3101 (2022).
95. Shan, L. et al. A sensory memory processing system with multi-wavelength synaptic-polychromatic light emission for multi-modal information recognition. *Nat. Commun.* **14**, 2648 (2023).
96. Wang, Y.-K. et al. Long-range order enabled stability in quantum dot light-emitting diodes. *Nature* **629**, 586–591 (2024).
97. Sun, H. et al. The development of customized perovskite photodetectors. *Nat. Electron.* **8**, 1170–1181 (2025).
98. Li, C. et al. Ultrafast and broadband photodetectors based on a perovskite/organic bulk heterojunction for large-dynamic-range imaging. *Light Sci. Appl.* **9**, 31 (2020).
99. Hou, Y. et al. Retina-inspired narrowband perovskite sensor array for panchromatic imaging. *Sci. Adv.* **9**, eade2338 (2023).
100. Chu, D. et al. Lattice engineering for stabilized black  $\text{FAPbI}_3$  perovskite single crystals for high-resolution x-ray imaging at the lowest dose. *Sci. Adv.* **9**, eadh2255 (2023).

## Author contributions

W.Y., X.Y., and R.S. researched most of the data and wrote the draft. L.Z., R.S., Y.F., M.L., X.W., R.Z., and C.P. commented the manuscript. W.Y., X.Y., R.S., L.Z., and D.L. revised the manuscript. D.L. supervised the project.

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## Competing interests

The authors declare no competing interests.

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