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RESEARCH ARTICLE

Monolithic 2D Synapse-Neuron Integration via Defect-Engineered h-BN for Energy-Efficient Neuromorphic Computing

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ABSTRACT

Neuromorphic computing offers a route to overcome the von Neumann bottleneck by emulating coupled synaptic and neuronal functions. However, monolithic integration of these components remains challenging due to mismatches in material platforms, operating mechanisms, and device architectures. Here, we exploit defect-engineered hexagonal boron nitride (h-BN) to realize a monolithic synapse–neuron platform within a unified 2D materials system. An optoelectronic synapse based on a MoS_2/h-BN heterostructure and a filamentary neuron formed in an Ag/h-BN/graphite stack are spatially separated yet electrically coupled through a shared h-BN dielectric. Under ultraviolet illumination and gate bias, defects in h-BN and at the h-BN/SiO_2 interface are activated, enabling tunable, reversible, and retained multilevel conductance that emulates both short- and long-term plasticity. The synapse supports 8-bit-equivalent accessible conductance updating and 6-bit retained state separability, enabling CIFAR-10 inference comparable to software baselines. Volatile h-BN filaments provide threshold switching and leaky integrate-and-fire dynamics. In a one-neuron–one-synapse configuration, gate-tunable current compliance and intrinsic neuronal thresholding suppress redundant low-weight synaptic signals, reducing the estimated synaptic read-current contribution by >80% with negligible accuracy degradation. This work establishes a proof-of-concept shared-h-BN platform for physically coupled synaptic storage and neuronal activation, providing a device-level route toward energy-efficient neuromorphic hardware.

1 | Introduction

The human brain performs complex cognitive functions, including perception, learning, and memory, with an ultralow power consumption of approximately 20 W while executing on the order of 10^{16} parallel operations per second [1, 2]. This extraordinary efficiency originates from a massively parallel architecture in which synapses and neurons operate in a tightly coupled and cooperative manner [3, 4]. Synapses serve as adaptive elements for information storage and weight modulation [5], whereas neurons function as nonlinear units that integrate, threshold, and transmit signals [6]. Through their continuous and reciprocal interaction, synaptic weighting and neuronal activation are intrinsically co-optimized, enabling highly energy-efficient information processing [4]. Inspired by this principle, neuromorphic hardware integrating synaptic memory with neuronal dynamics

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has emerged as a promising approach to address the growing computational and energy demands of artificial intelligence [7–9]. However, most existing systems physically separate synaptic and neuronal functions into distinct device modules, overlooking their inherently coupled and co-evolving nature in biological systems [6, 10–19]. This separation fundamentally limits energy efficiency, scalability, and biomimetic fidelity.

Two-dimensional (2D) materials provide a compelling platform for high-density neuromorphic devices due to their atomic thickness, excellent electrostatic tunability, and compatibility with heterogeneous integration [9, 20, 21]. Their reduced dimensionality enables efficient carrier transport and strong gate control [9, 22, 23], while their sensitivity to electrical and optical stimuli supports multiphysics modulation [10, 12]. Moreover, the availability of metallic, semiconducting, and insulating 2D materials allows versatile construction of van der Waals heterostructures [24–26]. Leveraging these attributes, substantial progress has been achieved in 2D neuromorphic devices. Semiconducting channels have enabled electrical synapses [27], as well as optical [28, 29] and optoelectronic synapses [10, 12] that emulate multimodal plasticity. In parallel, insulating materials such as hexagonal boron nitride (h-BN), combined with active electrodes, have been used to realize artificial neurons exhibiting threshold switching and all-or-none firing characteristics [30, 31]. Alternative strategies employ ferroelectric effects or reconfigurable heterostructures to toggle between synaptic and neuronal functionalities within a single device [32]. Despite these advances, most studies focus on isolated implementation of either synaptic or neuronal behavior [10, 12, 15. 16, 33], or rely on mode switching within a single device [26, 31, 32], rather than establishing a physically integrated platform that enables their cooperative operation.

When synaptic and neuronal functions are implemented in separate devices, two critical challenges arise. First, memristive neurons typically require external current compliance circuits to prevent hard breakdown, increasing system complexity and energy overhead [30, 34, 35]. Second, synaptic arrays generate abundant low-weight signals that still contribute to synaptic read current during inference, although they contribute little to inference accuracy. These issues originate from a fundamental mismatch in material systems and operating mechanisms between artificial synapses and neurons [26, 31, 32]. Specifically, synaptic devices favor field-effect modulation in semiconductors to achieve retained, analog, and multilevel weight tuning, whereas neuronal devices rely on electrochemical filament formation in insulating media to realize threshold switching and nonlinear firing [5, 20].

Here, we address this mismatch by exploiting the multifunctionality of hexagonal boron nitride to construct a physically coupled synapse–neuron system within a unified 2D materials platform. By spatially partitioning functionalities on a shared h-BN dielectric layer, we monolithically integrate an optoelectronic MoS_2/h-BN synapse with a filamentary Ag/h-BN/graphite neuron. Ultraviolet-assisted defect activation in h-BN and at the h-BN/SiO_2 interface enables controllable charge trapping and retained multilevel conductance modulation, supporting synaptic plasticity. Concurrently, conductive filaments in h-BN produce threshold switching and leaky integrate-and-fire dynamics. This monolithic integration provides the structural basis for one-neuron–one-synapse (1N1S) coupling, in which the synaptic transistor stabilizes neuronal operation through gate-tunable current compliance, while neuronal thresholding suppresses redundant low-weight synaptic-current pathways. Based on the fraction of synaptic pathways that remain active after threshold filtering, the estimated synaptic read-current contribution is reduced by over 80% with negligible accuracy degradation. These results show that the shared-h-BN 1N1S device can combine local current compliance with low-weight signal filtering in a physically integrated 2D platform.

2 | Results and Discussion

2.1 | Device Structure

Figure 1a schematically illustrates the biological neuron–synapse architecture that motivates the design of neuromorphic hardware. In biological neural systems, dendrites receive and preprocess input signals from upstream neurons [36, 37], while the soma integrates these inputs both spatially and temporally to determine whether an action potential is generated [26]. Once the firing threshold is exceeded, the axon propagates the electrical spike to downstream neurons. Emulating such functionality in artificial systems requires neuronal devices that exhibit pronounced threshold nonlinearity together with a high ON/OFF ratio to ensure reliable firing and clear state discrimination. Meanwhile, synapses serve as the communication links between neurons by modulating connection weights and storing activity history. Consequently, artificial synaptic devices must provide controllable and reversible conductance modulation, slowly relaxing conductance states, and distinguishable programmable conductance levels to enable high-fidelity information encoding and transmission.

Figure 1b presents an optical micrograph of the monolithically integrated synapse–neuron device constructed from a multilayer h-BN van der Waals heterostructure, while Figure 1c depicts its corresponding 3D atomic configuration. Although Figure 1b,c appear visually different because of the different electrode geometries, they correspond to the same equivalent circuit configuration. A scanning electron microscopy (SEM) overview is provided in Figure S1a. The synaptic unit is realized using a MoS_2/h-BN van der Waals phototransistor, fabricated by transferring MoS_2 onto the h-BN substrate. Extended source and drain electrodes confine carrier transport within the channel region, ensuring stable and reproducible synaptic operation. For the neuronal unit, multilayer graphite is introduced beneath the h-BN layer as a metal-like bottom electrode, while an Ag/Au bilayer serves as the top electrode. The incorporation of the graphite layer sharpens the switching characteristics and suppresses excessive Ag diffusion into the SiO_2 substrate. In addition, the graphite layer transforms the conventional vertical metal–insulator–metal geometry into a planar structure, thereby simplifying device fabrication and facilitating large-scale integration [38]. The synaptic and neuronal components are monolithically integrated within the same h-BN material platform and electrically coupled through series-connected electrodes. The Ag/Au electrode stack is deliberately designed such that Ag functions as the active electrode responsible for conductive-filament formation, whereas the Au capping layer prevents Ag oxidation and improves

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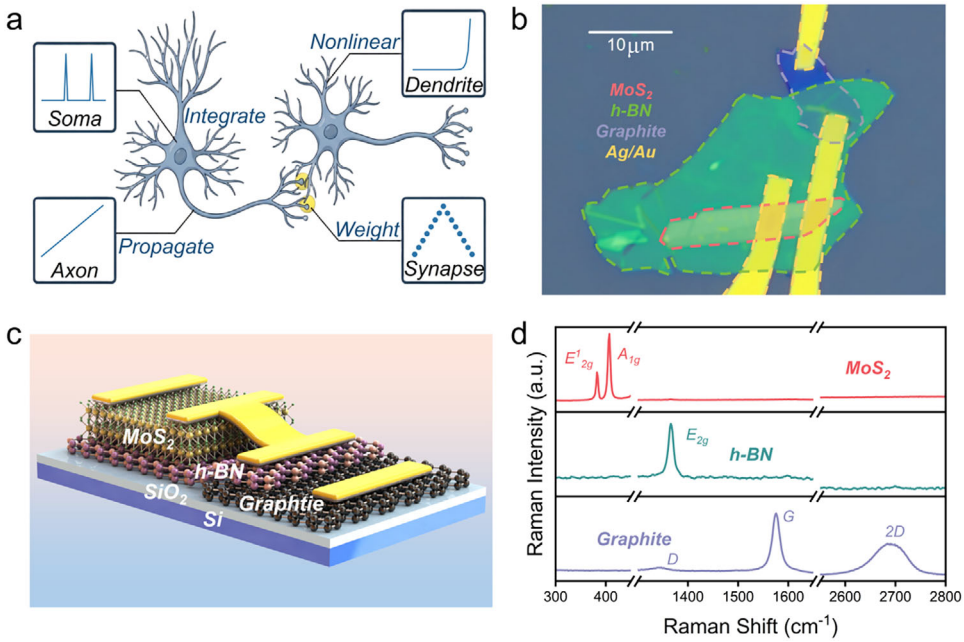


FIGURE 1 | Device structure and morphological characterization. (a) Schematic of signal processing in a biological synapse–neuron circuit and the corresponding electrical attributes targeted for neuromorphic emulation. (b) Optical micrograph of the monolithically integrated synapse–neuron device based on a multilayer h-BN van der Waals heterostructure. (c) Atomistic schematic of the fabricated device. (d) Raman spectra of MoS_2, h-BN, and multilayer graphite, confirming the material quality used for device integration.

electrode stability. Previous studies have reported pronounced Ohmic contact at the Ag/MoS_2 interface, attributed to weak interfacial reactions, favorable wettability, and dense contact morphologies [39, 40]. Consistent with these reports, several of our devices also exhibit clear Ohmic characteristics (Figure S2). The electrode configuration is further verified by cross-sectional SEM imaging (Figure S1b) and energy-dispersive x-ray spectroscopy (EDX) elemental mapping (Figure S1c). The material quality of MoS_2, h-BN, and graphite is confirmed by Raman spectroscopy (Figure 1d), while Figure S3 summarizes the corresponding EDX elemental analysis and atomic force microscopy (AFM) measurements used to determine the thickness of each constituent layer.

2.2 | Artificial Synapse

Synaptic plasticity forms the physical basis of learning and memory in biological systems by enabling activity-dependent modulation of synaptic connection strength. Artificial synaptic devices must therefore support controllable, reversible, and retained modulation of synaptic weights over a wide dynamic range. To meet these requirements, we develop an optoelectronic doping strategy [41, 42] enabled by the synergistic action of UV illumination and gate bias (V_{gs}). As schematically illustrated in Figure 2a, reversible n-type and p-type doping can be achieved simply by reversing the polarity of V_{gs} under low-intensity UV illumination.

Under illumination, electron–hole pairs are generated in the MoS_2 channel, while defect states within the h-BN layer and at the h-BN/SiO_2 interface become activated. The vertical electric field imposed by V_{gs} drives the photogenerated carriers to tunnel into the h-BN layer, where they are captured by defect states distributed within the h-BN layer and at the h-BN/SiO_2 interface, forming polarity-dependent trapping pathways. This trapping process produces an effective electrostatic doping effect in the MoS_2 channel. Specifically, when a negative V_{gs} is applied, photogenerated holes are preferentially trapped in both h-BN bulk defects and interfacial states. The resulting built-in vertical electric field shifts the MoS_2 Fermi level toward the conduction band, increasing the electron concentration and thereby inducing n-type doping. Reversing the gate bias favors electron trapping associated with interfacial defect states and consequently drives the channel toward p-type doping. The corresponding band-diagram evolution is summarized in Figure 2b. This optoelectronic doping mechanism therefore provides a programmable route for reversible conductance modulation, forming the physical basis of artificial synaptic operation.

The doping–relaxation current–time (I–t) characteristics in Figure 2c characterize the post-programming evolution of the optoelectronically doped conductance state. The measurement was performed in ambient air at room temperature with a fixed drain–source voltage (V_{ds}) of 0.5 V. In the initial stage, no gate bias or illumination was applied, and the drain–source current (I_{ds}) remained stable at approximately 0.05 μA. The V_{gs} of −30 V was then applied together with 255 nm UV illumination (2 mW cm^{-2}). The negative gate bias initially depletes the n-type MoS_2 channel, leading to an immediate decrease in I_{ds}, while the subsequent defect-assisted charge trapping under combined UV illumination and gate bias gradually enhances the channel conductance. After removal of both the optical and electrical stimuli, the device returns to the dark readout condition at zero gate bias, and I_{ds} increases to approximately 2.5 μA. The current then gradually relaxes with time but remains 5 times higher than the initial state

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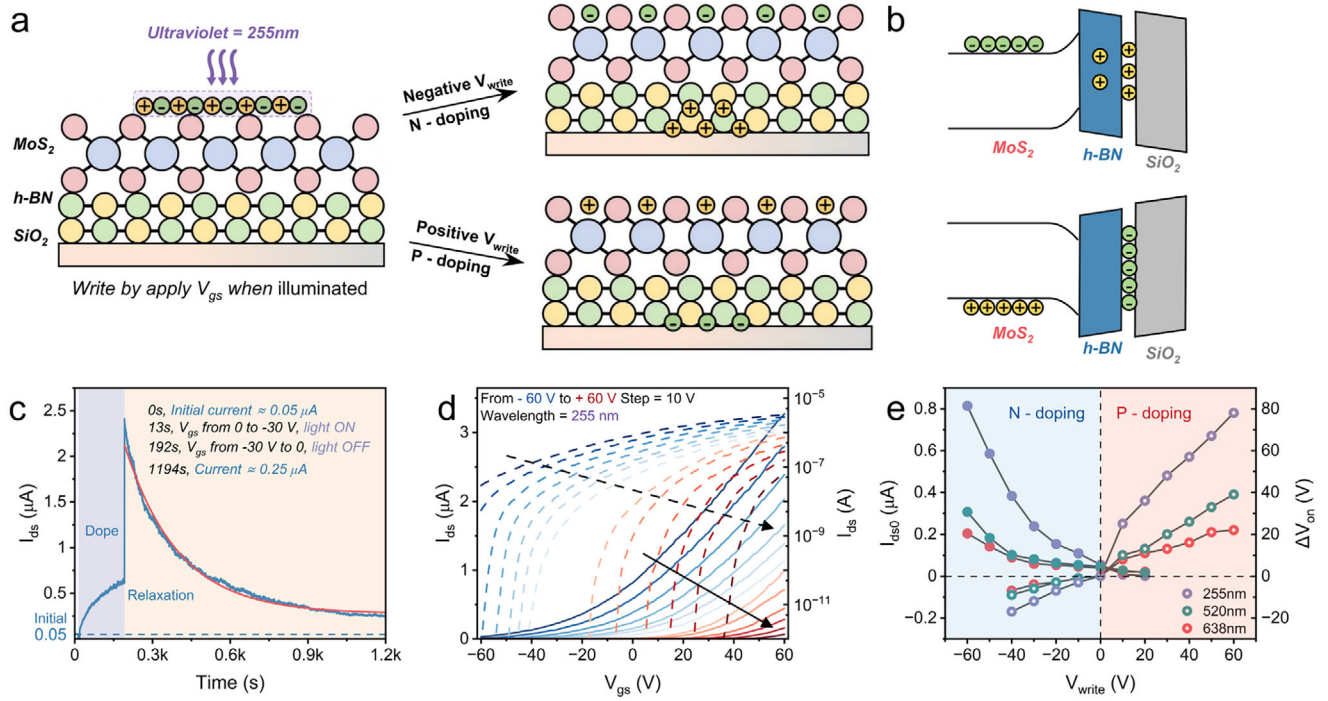


FIGURE 2 | Optoelectronic doping mechanism and conductance modulation of the artificial synapse. (a) Plan-view atomistic schematic of the MoS_2/h-BN/SiO_2 region illustrating the separation and migration of photogenerated carriers under V_{gs} of opposite polarities during optoelectronic doping. (b) Schematic band diagram of the MoS_2/h-BN/SiO_2 interface after doping. (c) Doping–relaxation I–t characteristics showing post-stimulus retention and gradual relaxation of the programmed conductance state in ambient air at room temperature. (d) Transfer characteristics measured at V_{ds} = 0.1 V after saturation doping under 255 nm UV illumination (2 mW cm^{-2}) with different V_{write}. Solid curves are shown on a linear scale and dashed curves on a logarithmic scale, revealing reversible reconfiguration of the conductance states by V_{gs} of opposite polarities. (e) Statistics of the extracted characteristic parameters I_{ds0} and ΔV_{on} from (d) and Figure S6 under different V_{write} values and illumination wavelengths; I_{ds0} (left axis) and ΔV_{on} (right axis) together indicate wide-dynamic-range and wavelength-dependent conductance modulation enabled by optoelectronic doping.

after 10^3 s, indicating retained conductance modulation. We further compared the retention behavior of another independently fabricated MoS_2/h-BN synaptic device under ambient air at room temperature, ambient air at 100°C, and vacuum at room temperature (Figure S4). These measurements were performed on a separate device to evaluate the environmental dependence of the post-programming relaxation behavior. The substantially faster relaxation at elevated temperature and the enhanced retention under vacuum suggest that the conductance relaxation process is jointly influenced by thermally activated charge detrapping and environmental adsorption/desorption processes.

To further characterize the programmable doping behavior, transfer characteristics were measured after saturating the device at different write voltages (V_{write}) followed by a 10 s relaxation period to minimize the influence of residual photocarriers. The measurements were performed at $V_{ds} = 0.1$ V with V_{gs} swept from −60 to 60 V for the pristine and n-type states, and from 60 to −60 V for the p-type states, using a step size of 1 V. The opposite sweep directions were deliberately chosen to avoid disturbing the established doping states by an initial gate bias of opposite polarity. As shown in Figure 2d, both linear and logarithmic plots clearly distinguish the n-type and p-type conductance states, confirming stable and reversible bidirectional doping. In contrast, a control MoS_2 device without the h-BN layer exhibits only a weak response under identical conditions (Figure S5a), highlighting the essential role of h-BN in enabling efficient charge trapping and electrostatic doping. Furthermore, a bottom-gated Au/h-BN/MoS_2/Au device without the SiO_2 interface (Figure S5b) shows a reduced but still observable n-type modulation, while the p-type response is largely suppressed. This comparison suggests that n-type doping involves contributions from both h-BN bulk defects and interfacial states, whereas p-type doping is more strongly associated with defect states at the h-BN/SiO_2 interface. The wavelength dependence of the optoelectronic doping process was further investigated using illumination at 520 and 638 nm with a fixed intensity of 50 mW cm^{-2} (Figure S6). Although reversible conductance modulation is observed at all wavelengths, the doping efficiency under 255 nm illumination is markedly higher, even at intensities nearly 25 times lower than those used at longer wavelengths. The much higher doping efficiency observed under 255 nm illumination likely arises because its photon energy exceeds the excitation threshold of defect states in both the h-BN bulk and the h-BN/SiO_2 interface, enabling efficient activation of multiple trapping channels. As a result, a large population of defect states can be activated, leading to substantially enhanced carrier trapping.

To quantitatively evaluate the achievable conductance modulation range, key parameters extracted from Figure 2d and Figure S6 are summarized in Figure 2e. The drain current at zero gate bias (I_{ds0}) and the shift in turn-on voltage (ΔV_{on}) are used as performance metrics, where V_{on} is defined as the gate voltage at which Ids first exceeds 10^{-12} A. After n-type doping at

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V_{write} = −60 V, I_{ds0} increases by approximately 15 times relative to the pristine state, whereas strong p-type doping suppresses I_{ds0} below the measurement limit. Meanwhile, ΔV_{on} reaches 78 V at V_{write} = 60 and −17 V at V_{write} = −40 V, indicating a wide tunability window (for V_{write} = −50 and −60 V, Von falls outside the measurement range and ΔV_{on} is therefore not extracted). Notably, most previously reported MoS_2 optoelectronic synapse devices employ 520 nm illumination due to the strong optical absorption of MoS_2 at this wavelength [43, 44]. In contrast, our wavelength-dependent experiments reveal that 255 nm illumination enables substantially higher doping efficiency even at ~25-fold lower optical intensity. This behavior indicates that the optoelectronic doping process is dominated by defect-state excitation in h-BN rather than by the intrinsic optical absorption of MoS_2. The higher photon energy of 255 nm illumination likely surpasses the excitation threshold of these defects, allowing a substantially larger number of trapping centers to participate in carrier trapping. Collectively, these results demonstrate that the MoS_2/h-BN synaptic device supports wide-range, low-energy, and reversible conductance modulation via optoelectronic doping.

As illustrated in Figure 3a, trains of UV and V_{gs} pulses are used to emulate inputs from two presynaptic neurons. In biological neural circuits, signals from multiple presynaptic neurons converge onto a postsynaptic neuron to generate a response. Analogously, the I_{ds} of the device serve as the electrical output representing the postsynaptic response strength. By tailoring pulse parameters, the synaptic weight can be continuously tuned, enabling multilevel conductance states for analog weight representation. Detailed analysis of the wide dynamic range enabled by the optoelectronic doping mechanism, together with a comparison to conventional synaptic devices, is provided in Figure S7 and Note S1. Building on this mechanism, pulse trains with identical amplitudes are used to generate nonuniform multilevel weight states, enabling bioinspired analog weight representation. To quantitatively assess the advantage of combined optoelectronic stimulation over purely optical excitation, 15 paired pulse measurements were performed on the same device, with all parameters kept identical except for the presence of electrical gating (Figure S8). The optoelectronic stimulation produces a response amplitude approximately three times larger than that obtained under purely optical excitation, indicating that the synergistic optoelectronic stimulation enables larger and more distinguishable weight updates. To further investigate short-term synaptic plasticity associated with transient information processing, paired-pulse facilitation (PPF) was examined. PPF is characterized by an enhanced response to a second stimulus applied shortly after the first, with the facilitation ratio decreasing as the interpulse interval increases. The inset of Figure 3b schematically illustrates the current response under two consecutive optoelectronic pulses. Here, A_1 and A_2 denote the peak current increments induced by the first and second pulses relative to the initial current, respectively, and the facilitation ratio is defined as PPF = $(A_2/A_1) \times 100\%$. The dependence of PPF on the interpulse interval is well described by a double-exponential decay across 12 independent measurements, yielding time constants of $\tau_1 = 1.3$ s and $\tau_2 = 9.1$ s. These characteristic times correspond to fast and slow facilitation components that closely resemble those observed in biological synapses. Beyond transient plasticity, the transition from short-term memory (STM) to long-term memory (LTM) was further investigated under repeated stimulation. By systematically varying the light intensity, V_{gs} pulse amplitude, pulse number, frequency, and duty cycle of the optoelectronic pulses (Figure S9), the device conductance can be gradually programmed into highly distinguishable states, enabling the emulation of STM-to-LTM transitions in biological synapses.

Based on these results, further reducing the pulse width allows finer and more controllable conductance evolution from the initial to the saturated state, thereby increasing the number of accessible weight levels. Considering practical constraints such as the minimum readout interval of the measurement system, a pulse width of 0.15 s was selected. Under combined optoelectronic stimulation with a light intensity of 2 mW cm^{-2} and a −10 V V_{gs} pulse (inset of Figure 3c), the conductance evolution can be discretized into 256 accessible incremental update levels, corresponding to an 8-bit-equivalent programmable conductance resolution under the present pulse-programming and readout protocol, as shown in Figure 3c. Similarly, applying a 10 V V_{gs} pulse with a width of 1.2 s enables 256 accessible decremental conductance-update levels. Further shortening the pulse width is expected to enable even higher weight precision. Similar multilevel conductance modulation was also observed in three independently fabricated devices, supporting the device-to-device reproducibility of the synaptic weight programming behavior (Figure S10). Because the absolute current level varies among exfoliated-and-transferred MoS_2/h-BN devices, the reproducibility of synaptic programming is evaluated by the conductance-modulation trend and normalized response. To further evaluate retained state separability, we performed a 100 s retention test and normalized the measured conductance values into relative synaptic weights. As shown in Figure 3d, 64 normalized weight states remain ordered without crossing throughout the retention window, corresponding to 6-bit distinguishable retained states under the present measurement and processing conditions. Together, these results show that the device combines high programming resolution with retained multilevel separability over the tested retention window.

To evaluate the system-level impact of the accessible and retained weight precision, a CIFAR-10 image-classification task was implemented using a modified VGG11 architecture (Figure 3e). The network consists of five convolutional blocks incorporating convolution, batch normalization, and rectified linear unit (ReLU) activation, followed by max-pooling for feature extraction, and three fully connected (FC) layers for classification. Dropout layers were included to suppress overfitting. Training was conducted in software, while inference accuracy was evaluated after each epoch using quantized weights with different bit widths. Accordingly, we evaluated network performance using both 8-bit and 6-bit quantized weights, corresponding to the accessible programming resolution and the retained state separability extracted above, respectively. After each evaluation step, training resumed using full-precision weights, enabling direct assessment of the influence of quantization precision on network performance throughout the training process. As shown in Figure 3f, the 8-bit quantized network closely follows the software baseline during training and reaches a final accuracy comparable to the full-precision model. The 6-bit quantized network shows only a slight accuracy loss relative to the 8-bit case, indicating that the retained distinguishable states remain effective for network inference in the present task. These results suggest that the 256 accessible conductance-update levels can support

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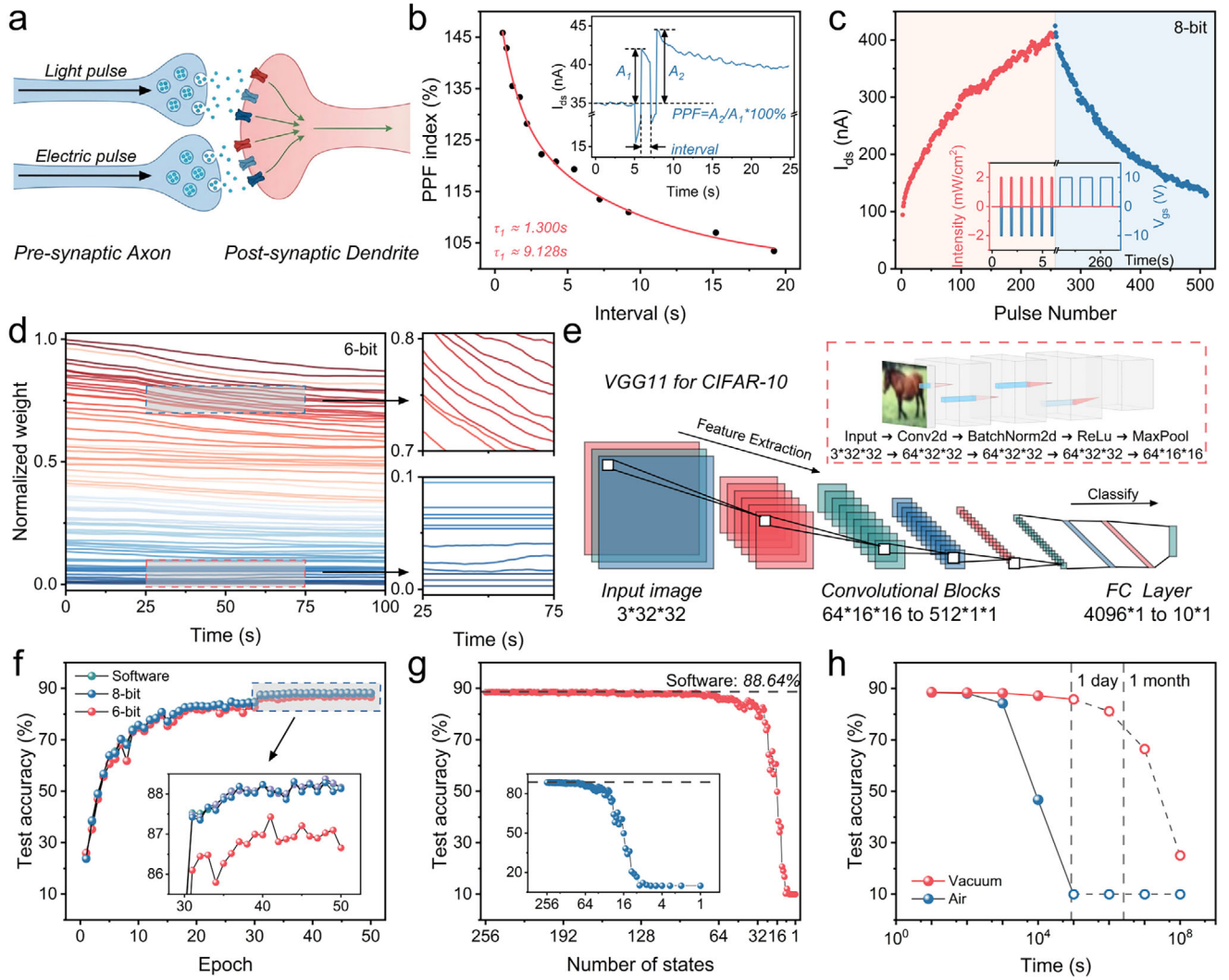


FIGURE 3 | Functional demonstrations and network evaluation of the optoelectronic synapse. (a) Schematic illustrating the convergence of multiple presynaptic neurons onto a single postsynaptic neuron in biological neural systems, and its emulation using the optoelectronic synaptic device. (b) PPF characteristics of the artificial synapse, showing exponential decay of the facilitation ratio as a function of the interpulse interval; the inset depicts a representative PPF response at an interval of 1.2 s. (c) Multilevel synaptic weight programming showing 256 accessible conductance-update levels under the present pulse-programming and readout protocol. (d) Retention-based state-separability analysis showing 64 normalized weight states that remain ordered without crossing during a 100 s retention window. (e) Schematic of the convolutional neural network used for CIFAR-10 image classification, based on a modified VGG11 architecture. (f) CIFAR-10 classification accuracy during training using software-based, 8-bit quantized, and 6-bit quantized weights. The inset highlights the final accuracy difference between the 8-bit and 6-bit quantized models after training convergence. (g) Test accuracy of the trained network as a function of the usable conductance-state number. The inset shows the same accuracy trend plotted on a logarithmic state-number axis. (h) Test accuracy of the trained network as a function of relaxation time after incorporating the experimentally extracted weight-retention factors under air and vacuum conditions.

high-resolution weight mapping, while the 64 distinguishable retained states can still provide sufficient effective precision for CIFAR-10 inference with limited accuracy degradation. To further examine how the usable number of conductance states affects network performance after training, we progressively reduced the number of available weight states through post-training quantization and evaluated the corresponding CIFAR-10 accuracy (Figure 3g) and loss (Figure S11). The network maintains accuracy close to the software baseline when the usable state number remains above approximately 64. However, when the number of states is reduced below several tens, the test accuracy decreases rapidly, accompanied by a sharp increase in loss. The inset of Figure 3g further presents the same accuracy trend on a logarithmic state-number axis, more clearly showing the rapid performance collapse at low state numbers. These results indicate that the network remains tolerant to moderate reductions in usable conductance-state number, but becomes unstable when the remaining states are insufficient to represent the trained weights with adequate precision.

We further evaluated how the measured conductance relaxation affects network inference over time. Based on the experimentally measured relaxation characteristics under air and vacuum conditions, time-dependent normalized weight-retention factors were

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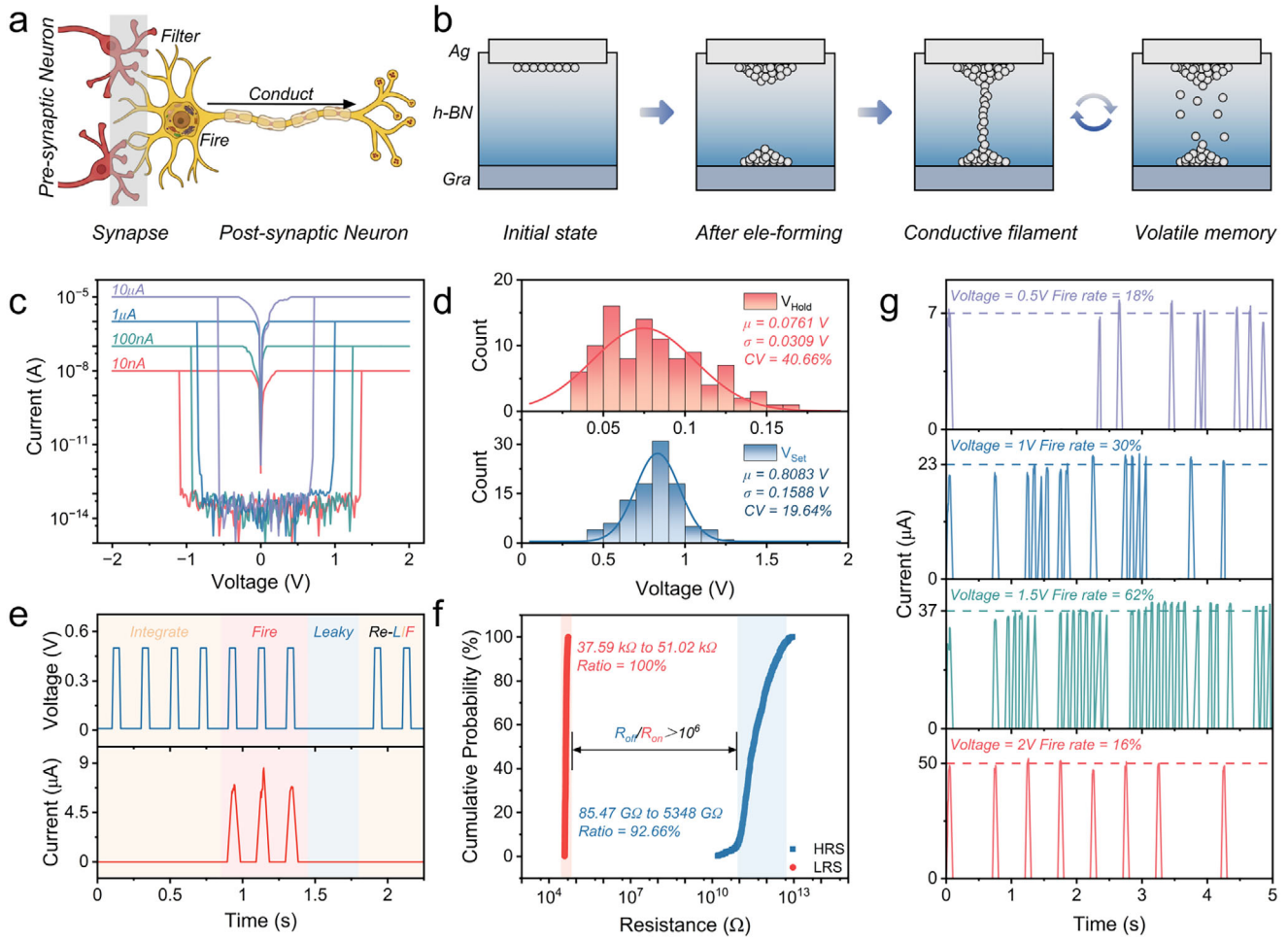


FIGURE 4 | Artificial neuron based on conductive filaments. (a) Schematic illustration of the operating principle of a biological neuron as a functional reference. (b) Schematic of volatile conductive filament formation and rupture in the Ag/h-BN/graphite structure underlying the artificial neuron operation. (c) Nonlinear output current responses of the artificial neuron to linear input voltage sweeps under different I_C, revealing a pronounced ON/OFF ratio. (d) Cycle-to-cycle switching statistics of V_{Set} and V_{Hold} extracted from 100 consecutive bidirectional voltage sweeps at the fixed-I_C of 1 μA with a fixed waiting interval between adjacent cycles. (e) Emulation of LIF neuronal behavior. (f) Resistance distributions of HRS and LRS under consecutive pulse stimulation. (g) Output current responses to consecutive voltage pulses with different amplitudes (0.5, 1, 1.5, and 2 V).

extracted (Figure S12) and applied to the trained convolutional and fully connected weights. As shown in Figure 3h, the network accuracy decreases rapidly under air conditions because of fast weight relaxation, whereas the slower relaxation under vacuum maintains higher inference accuracy over longer times, including the one-day to one-month range. This result directly links device-level retention degradation to network-level accuracy loss and highlights the importance of improving environmental stability for long-term neuromorphic inference. Together, these results highlight the potential of the MoS_2/h-BN optoelectronic synaptic device for high-precision neuromorphic computing.

2.3 | Artificial Neuron

As illustrated in Figure 4a, biological neurons process information by filtering and integrating upstream inputs and generate action potentials only when the integrated signal exceeds a threshold. Accordingly, an artificial neuron should exhibit pronounced threshold nonlinearity together with a high ON/OFF ratio to ensure reliable firing and clear state discrimination. To satisfy these requirements, we integrate an Ag/h-BN/graphite memristive neuron on the opposite side of the device, where neuronal firing behaviors can be tuned by controlling the compliance current (I_C), as schematically illustrated in Figure 4b. In the pristine state, partial Ag pre-diffusion occurs at the h-BN interface during top-electrode deposition, while the interfacial morphology remains relatively uniform. During the forming process, a positive bias applied to the Ag electrode oxidizes Ag atoms into Ag^+ ions, which subsequently migrate along the van der Waals interlayers of h-BN under the electric field. These ions can be trapped or guided by defect sites and interlayer pathways in h-BN, progressively accumulating to form conductive filaments. After forming, residual Ag species remain distributed within the h-BN layer and near the graphite interface, enabling reversible filament growth and rupture under opposite-polarity voltage sweeps and thereby producing bipolar memristive switching with a large ON/OFF ratio [45]. On this basis, a bidirectionally conducting artificial neuron can be realized following a unipolar forming process [46]. During repeated voltage sweeps, the magnitude of I_C regulates charge transport through the filaments as well as the associated local Joule heating, thereby modulating filament

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morphology and stability and leading to distinct electrical behaviors corresponding to different neuronal firing modes [47, 48]. In this work, Figure 4 focuses on the volatile regime under small I_C, where the filaments formed during the forward sweep are thin and unstable and tend to rupture during the backward sweep, requiring reformation in subsequent cycles (Figure 4b). By contrast, larger I_C values promote thicker and more stable filaments that persist across cycles and result in nonvolatile switching behavior, whereas removing the current compliance leads to excessive Joule heating and catastrophic filament collapse (Figure S13). Further discussion of these regimes is provided in Note S2; the following analysis therefore concentrates on neuronal firing emulation in the volatile mode. To further verify the role of the active metal electrode, we fabricated control devices in which the Ag electrode was replaced by inert Au while keeping the h-BN/graphite structure unchanged (Figure S14). In contrast to the Ag/h-BN/graphite neuron, the Au/h-BN/graphite control devices do not show stable low-voltage threshold switching, and some devices remain non-switching even under much higher voltage sweeps. This comparison confirms that the active Ag electrode is essential for the observed filamentary switching behavior, supporting the Ag-ion-migration-mediated conductive-filament mechanism.

Figure 4c presents the current response under linear voltage sweeps from −2 to 2 V with a step size of 0.02 V at different I_C values. At low input voltages, conductive filaments have not yet formed, and charge transport is dominated by unstable tunneling and defect-assisted conduction, corresponding to a leakage-dominated high-resistance state (HRS). When the input voltage exceeds the threshold voltage (V_{Set}), Ag filaments are formed and establish a filamentary conduction pathway, switching the device into a low-resistance state (LRS). These I–V characteristics confirm that, after forming, the artificial neuron exhibits bidirectional conduction with a sharp threshold nonlinearity. In addition, the representative data in Figure 4c illustrate the threshold-switching behavior measured under different I_C. It should be noted that I_C does not directly affect V_{Set} within a single voltage sweep, because the compliance current becomes effective only after conductive-filament formation. Instead, I_C mainly limits filament growth after the threshold-switching event and therefore regulates the morphology and stability of the formed filament. During repeated cycling, the filament morphology and residual Ag configuration left from the current cycle can further influence the ease of filament reformation in subsequent cycles, leading to history-dependent variation in the extracted apparent V_{Set}. To further clarify this point, we performed repeated switching measurements under both fixed-I_C and mixed-I_C protocols. For the fixed-I_C test, the device was measured for 100 consecutive bidirectional sweeps at $I_C = 1\,\mu A$, with a fixed waiting interval between adjacent cycles to allow partial device recovery. For comparison, mixed-I_C measurements were also performed, including 100 unidirectional sweeps and 100 bidirectional sweeps without a waiting interval between cycles. Figure 4d shows the statistical results obtained under the fixed-I_C protocol, while the corresponding raw switching curves, together with the raw data and statistical results from the mixed-I_C tests, are provided in Figure S15. From the histograms in Figure 4d, the mean V_{Set} and V_{Hold} under the fixed-I_C protocol are extracted to be 0.8083 and 0.0761 V, respectively, with corresponding CV (coefficients of variation) of 19.64% and 40.66%. Compared with the mixed-I_C results shown in Figure S15 (CVs of 34.97% and 48.17% for V_{Set} and V_{Hold}, respectively), the fixed-I_C measurement exhibits smaller CV values, indicating improved cycle-to-cycle stability and repeatability under a standardized operating condition. This comparison indicates that fixed-condition operation provides more reproducible switching statistics than the mixed-I_C test. Here, V_{Hold} is defined as the voltage at which the device current begins to decrease significantly below I_C due to spontaneous filament rupture. Unlike some previously reported volatile devices that require a finite sustaining voltage, the present device exhibits an almost zero sustaining voltage and spontaneously relaxes to the HRS once the external bias is removed. Our previous embedded-atom method (EAM) molecular dynamics simulations indicate that, in the volatile regime characterized by thin and unstable filaments, retention of the LRS does not require an additional sustaining voltage; importantly, this behavior does not imply nonvolatility [34]. This mechanism differs fundamentally from the nonvolatile regime (Figure S13a), where the current decays much more rapidly during the backward sweep, indicating that filament rupture is dominated by spontaneous structural collapse rather than gradual voltage-driven dissolution. Such spontaneous relaxation closely resembles the natural recovery process following neuronal firing in biological systems. Measurements from five independently fabricated devices show filamentary threshold switching within a similar voltage window, with mean V_{Set} values of 0.85–0.92 V and mean V_{Hold} values of 0.1–0.2 V, supporting the reproducibility of the average switching behavior while also revealing device-to-device variation (Figure S16).

Taking advantage of the intrinsic volatility in the small-I_C regime, we emulate the classical leaky integrate-and-fire (LIF) neuron model without applying an external reset voltage (V_{reset}), as shown in Figure 4e. In this configuration, consecutive voltage pulses represent incoming stimuli. During the integrate phase, prior to filament formation, the pulses do not trigger a firing response. Once a conductive filament forms, the device enters the fire phase and produces a pronounced current response to subsequent pulses. When the pulse train is removed, the filament ruptures spontaneously due to intrinsic volatility, resetting the device to the non-firing state without the need for an explicit reset pulse. Reapplying the pulse train returns the device to the integrate phase. Importantly, even without interrupting the pulse train, the neuron can still exhibit natural leakage during the interpulse intervals owing to the volatility of the conductive filaments. Figure 4f therefore employs a continuous pulse train and summarizes the resistance distributions of the HRS and LRS under uninterrupted pulsed operation. Under repeated pulse cycling, the ON/OFF ratio between the HRS and LRS remains on the order of 10^6. Although this value is slightly lower than that obtained from quasi-static sweeps (Figure 4c), due to residual Ag species that elevate the HRS current during pulse cycling, it remains sufficiently large to reproduce the all-or-none firing characteristic of biological neurons. The HRS shows larger dispersion because of unstable tunneling, defect-assisted transport, and measurement noise, whereas the LRS remains comparatively stable owing to conduction through metallic filaments. Figure 4g further reveals a non-monotonic dependence of firing behavior on pulse amplitude. Increasing the pulse amplitude from 0.5 to 1.5 V enhances the firing probability, whereas amplitudes exceeding 2 V significantly suppress firing.

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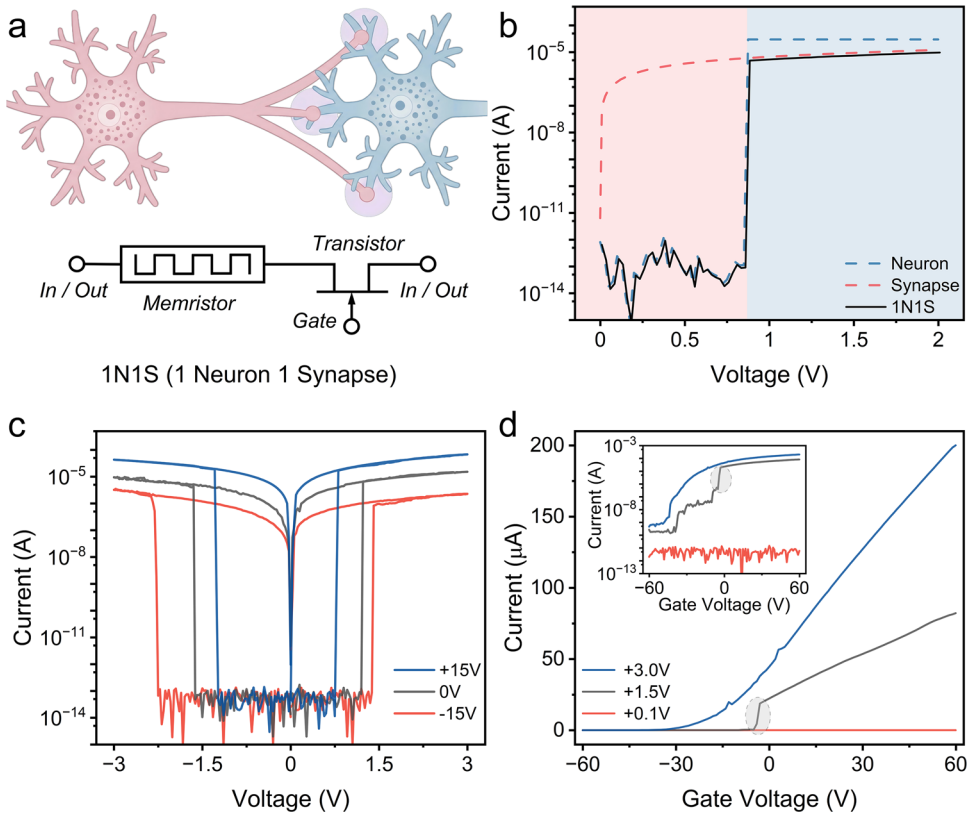


FIGURE 5 | Electrical characteristics of the 1N1S structure. (a) Schematic of the 1N1S architecture, motivated by the series coupling of synapses and neurons in biological nervous systems, together with the corresponding equivalent circuit model. (b) The 1N1S architecture enables stable neuronal operation without external current compliance circuitry by exploiting the intrinsic current-limiting behavior of the synaptic transistor. (c) Output characteristics of the 1N1S device under different V_{gs}, showing gate-tunable modulation of neuronal V_{Set} via voltage partitioning. (d) Transfer characteristics of the 1N1S device measured at different input bias voltages, plotted on a linear scale. The inset shows the same data on a logarithmic scale, highlighting an ultra-steep turn-on and a low apparent subthreshold swing.

This suppression originates from the fact that thin filaments in the volatile regime are susceptible to Joule-heating-induced premature collapse at currents of only tens of μA, as illustrated in Figure S13. In contrast, filament rupture in the nonvolatile regime typically requires milliampere-level currents, highlighting the markedly different filament stability between the two operating modes. This response also suggests that volatile operation can emulate neuronal responses to extreme stimuli. Collectively, the Ag/h-BN/graphite neuron device exhibits pronounced threshold nonlinearity, a high ON/OFF ratio, and intrinsic self-resetting volatility, enabling faithful emulation of leaky integrate-and-fire neuronal dynamics without the need for external reset pulses.

2.4 | Integrated Synapse-Neuron Device

Although the device exhibits favorable biomimetic characteristics when operated independently as an artificial synapse and as an artificial neuron, such a decoupled configuration still imposes intrinsic system-level limitations. In particular, the neuronal element typically requires peripheral current-compliance circuitry for stable operation, while the synaptic implementation contains a disproportionately large population of low-weight states that contribute little to inference accuracy (Figure 6a). These limitations motivate the development of an integrated architecture in which synaptic weighting and neuronal activation are physically and functionally coupled. Figure 5a presents the 1N1S architecture formed by serially integrating a synaptic transistor with a memristive neuron. Although this configuration bears structural similarity to conventional 1T1R schemes used in high-density nonvolatile memory arrays [53], its design principle and functional role are fundamentally different. Rather than acting as an access selector, the transistor in the present architecture functions as an active synaptic element whose field-effect tunability is directly utilized, while the memristor provides a threshold-type nonlinear neuronal response. Through this series coupling, the synaptic and neuronal units interact synergistically at the physical level, enabling device-level cooperative functionalities that cannot be achieved when the two elements operate independently.

Artificial neuron devices, including most conductive-filament memristors, typically require external current compliance to prevent irreversible degradation caused by Joule-heating-induced filament rupture (Figure S13). Allocating such circuitry to every neuron would substantially increase array-level overhead. In the proposed 1N1S architecture, however, the synaptic transistor intrinsically provides a tunable current-limiting function. As illustrated schematically in Figure 5b, the neuron dominates current regulation at low bias, whereas the synaptic transistor progressively clamps the current at higher bias. This cooperative current regulation effectively suppresses filament overheating

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and melting in the neuronal element even under large applied voltages, thereby eliminating the need for external compliance circuitry. Based on this mechanism, linear voltage sweeps were performed on the 1N1S structure under different V_{gs}, as shown in Figure 5c. Owing to the pronounced gate-tunable conductance of the synaptic transistor, the effective series resistance can be continuously adjusted, thereby modulating the voltage division between the synapse and the neuron under a fixed input bias. Consequently, the voltage drop across the neuronal element becomes tunable, leading to a gate-controlled neuronal switching threshold V_{Set}. Importantly, the multilayer graphite bottom electrode beneath the neuron effectively shields the neuronal element from the synaptic gate field, as confirmed by the absence of measurable neuronal-current modulation when sweeping V_{gs} in a preset nonvolatile state under low read bias (Figure S17). The same series-interaction mechanism also produces a transfer characteristic with an ultra-steep apparent turn-on (Figure 5d). When measured in a transistor-like configuration by sweeping V_{gs} under different input biases, the response can be divided into three regimes. At low input bias, the neuronal element remains below its threshold, and the current is strongly suppressed. At intermediate bias, increasing V_{gs} enhances synaptic conductance and shifts the voltage partition until the neuron crosses its threshold, resulting in an abrupt turn-on. At high input bias, the neuron is effectively activated from the outset, and the transfer curve approaches that of the standalone synaptic transistor. This threshold-assisted transition yields an exceptionally small apparent subthreshold swing, potentially below the conventional thermionic limit, highlighting an additional system-level functionality enabled by the interactive 1N1S coupling. Collectively, the 1N1S architecture eliminates the neuron's reliance on external current-compliance circuitry, enables gate-tunable control of the neuronal activation threshold, and produces an ultra-steep apparent subthreshold swing, underscoring its practical potential for compact and energy-efficient neuromorphic integration.

Beyond providing intrinsic current compliance, the series-coupled 1N1S architecture also addresses a readout inefficiency in trained neural networks, where many low-magnitude synaptic weights contribute little to inference accuracy. Figure 6a shows the parameter distribution of the modified VGG11 network (Figure 3e) trained to a final test accuracy of 88.47%. Under 8-bit quantization, the network occupies 254 discrete weight values spanning the range from −4 to 3. Among the approximately 28 million total weights, nearly 20 million cluster at five near-zero levels (0, ± 0.02, and ± 0.04), as highlighted in the inset focusing on the range from −0.3 to 0.3. From a hardware perspective, this concentration of low-weight synapses can increase the synaptic read-current burden, because these synapses dominate the synapse device count while contributing minimally to inference accuracy. The 1N1S architecture intrinsically suppresses this low-weight redundancy through neuronal threshold nonlinearity. As illustrated in Figure 6b, under a fixed input voltage (State I), voltage division across the series-connected synapse and neuron keeps the neuronal element below its switching threshold V_{Set}, so the output current remains at the leakage level of the HRS. In State II, the synaptic conductance is increased through optoelectronic programming but still resides within the low-weight regime; the neuron therefore remains inactive, effectively filtering out weak synaptic inputs. Once the synaptic conductance increases further (State III), the voltage drop across the neuron reaches V_{Set}, triggering neuronal activation and allowing high-weight signals to propagate. In this manner, weak synaptic contributions are naturally suppressed, whereas high-weight pathways are preserved. Similar qualitative behavior is also observed under purely optical stimulation (Figure S18), although the modulation efficiency is lower than that obtained with optoelectronic stimulation.

Guided by this neuron-enabled thresholding behavior, we further evaluated a network-level weight-thresholding scheme in which parameters with magnitudes below a given threshold are set to zero (Figure 6c). The fraction of zeroed weights is used here to estimate the reduction in synaptic read-current contribution, while the corresponding test accuracy quantifies the performance cost. As the threshold increases from small values, a large fraction of weights can be eliminated with minimal accuracy degradation. At larger thresholds, however, the zeroing ratio increases only slightly while the test accuracy drops sharply and approaches the network-independent baseline (~10%). This trade-off therefore defines a practical operating window in which redundant weights can be removed without significantly compromising recognition performance. At an optimal threshold of 0.12 (corresponding to the suppression of 11 low-magnitude levels from −0.12 to 0.12), 82.11% of weights can be zeroed while the test accuracy decreases by less than two percentage points (Figure 6d). The remaining nonzero synapses therefore account for only 17.89% of the original network. In the series-coupled 1N1S architecture, currents from the "zeroed" synapses are suppressed by the neuronal threshold to the picoampere level, which is negligible compared with the ~100 nA currents in active synaptic pathways. Consequently, these synapses become effectively inactive, and device-level electrical power dissipation associated with synaptic currents is dominated by the remaining nonzero synapses. Under the optimal threshold condition, where 17.89% of the synaptic pathways remain active, the synaptic read-current contribution can be approximated as 17.89% of the original value. This estimate only accounts for the synaptic read-current component associated with active weight pathways during inference and does not include peripheral circuits or array-level addressing costs. Collectively, these results show that neuron-enabled nonlinear filtering can suppress more than 80% of low-weight synaptic-current pathways with minimal accuracy penalty, suggesting potential device-level energy savings in the synaptic readout path rather than constituting a complete system-level energy benchmark.

These device-level results clarify the functional role and practical scope of the present shared-h-BN 1N1S unit within neuromorphic hardware. Mature nonvolatile memory technologies, particularly vertical NAND flash, provide highly optimized platforms for large-scale neural-network implementation in terms of integration density, reliability, and manufacturing maturity [54–56]. In contrast, the present monolithically integrated 2D platform is not intended as a direct alternative to NAND-based hardware, but rather as a device-level platform for exploring physical coupling between synaptic storage and neuronal threshold activation within a shared material system. This local coupling enables gate-tunable current compliance and threshold-assisted suppression of low-weight synaptic-current pathways at the device level. At the same time, the current devices still rely on exfoliation-and-transfer fabrication, UV-assisted optoelectronic

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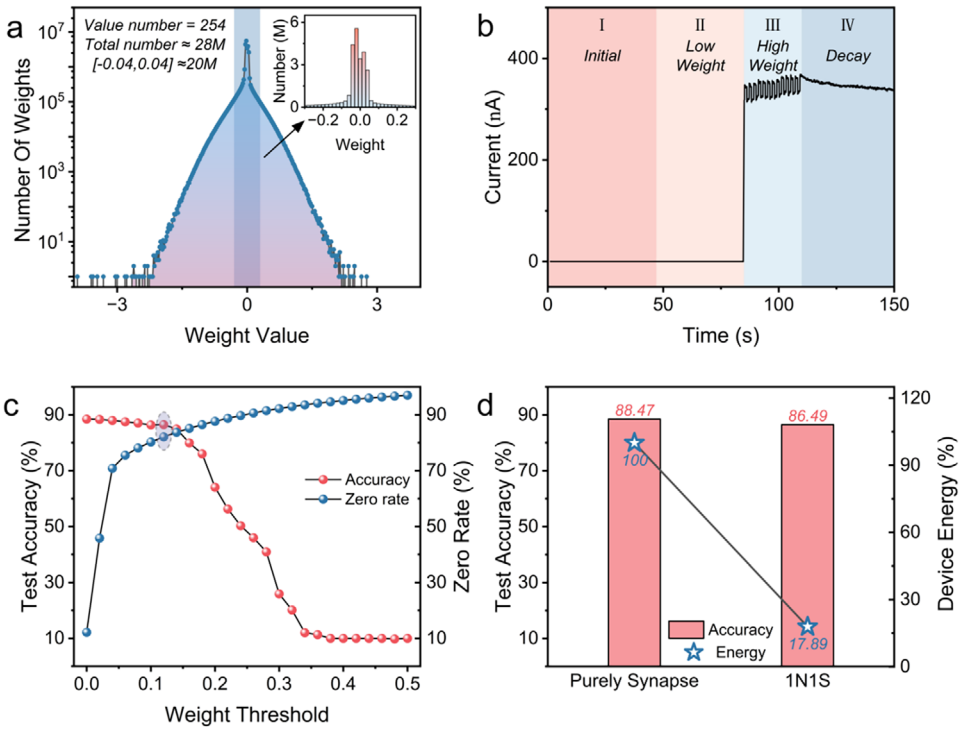


FIGURE 6 | Application of the 1N1S architecture in a neural network. (a) Distributions of weights and biases in the trained VGG11 neural network, plotted on a logarithmic vertical axis; the inset shows the parameter distribution within the range from −0.3 to 0.3 using a linear vertical axis. (b) Illustration of nonlinear filtering of low-weight synaptic signals enabled by the series-coupled 1N1S architecture. (c) Fraction of zeroed weights under different threshold values and the corresponding impact on network classification accuracy. (d) By filtering 11 low-weight levels, the network classification accuracy decreases from 88.47% to 86.49%, while the estimated synaptic read-current contribution from the remaining active pathways is reduced to 17.89% of the original value.

programming, and experimentally limited retention, and therefore require further optimization before practical array-level implementation. Future developments may involve wafer-scale 2D-material growth or transfer, lithography-compatible planar layouts, lower-voltage and electrically addressable programming schemes, transparent or h-BN-based encapsulation, and improved environmental and thermal stability [21, 57]. At the array level, shared or regional optical excitation combined with local electrical gate selection may provide a possible programming route, but practical implementation will require careful management of optical nonuniformity, non-selective excitation, parasitic coupling, sneak currents, half-select bias stress, and device-to-device variability [58–60]. Therefore, the present work should be viewed as a proof-of-concept device-level strategy for physically coupled synapse–neuron integration, rather than a fabrication-ready large-scale neuromorphic hardware platform. A comparison with representative neuromorphic systems is provided in Table S1 to further position the proposed architecture.

3 | Conclusions

In summary, we present a monolithically integrated synapse–neuron platform that enables the co-realization of synaptic plasticity and neuronal dynamics within a unified 2D material system. By harnessing the multifunctionality of hexagonal boron nitride (h-BN), an optoelectronic MoS_2/h-BN synapse and a conductive-filament-based Ag/h-BN/graphite neuron are spatially partitioned and monolithically integrated within a shared h-BN dielectric platform, establishing a physically coupled synapse–neuron unit. On the synaptic side, optoelectronic conductance programming enables reversible and wide-dynamic-range synaptic weight modulation with post-programming retention, supporting multilevel states and biologically relevant transitions from short-term to long-term plasticity. Network evaluation based on 8-bit-equivalent accessible conductance updating and 6-bit retained state separability shows CIFAR-10 classification accuracy comparable to software-based baselines, indicating effective synaptic weight representation. Retention-aware evaluation further shows that conductance relaxation can translate into time-dependent accuracy degradation, highlighting the importance of improving environmental stability for long-term inference. The neuronal device, governed by conductive filament dynamics in h-BN, demonstrates a high ON/OFF ratio, intrinsic self-resetting capability, and sharp threshold switching characteristics, enabling faithful emulation of leaky integrate-and-fire (LIF) behavior. In a series-configured one-neuron-one-synapse architecture, the synaptic transistor functions as a gate-tunable current compliance element, eliminating the need for external compliance circuitry while ensuring stable neuronal switching. Meanwhile, the inherent thresholding behavior of the neuron effectively filters low-weight synaptic inputs and suppresses redundant signal transmission. After filtering 11 low-weight levels, the network accuracy decreases from 88.47% to 86.49%, while the estimated synaptic read-current contribution from the remaining active pathways is reduced to 17.89% of

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the original value. This estimate refers only to the synaptic read-current during inference and does not include programming, peripheral-circuit, interconnect, neuron-switching, or array-addressing energy. Collectively, this work establishes a shared-h-BN device platform that physically couples synaptic storage and neuronal activation, providing a device-level route toward physically integrated neuromorphic hardware.

4 | Experimental Section

4.1 | Device Fabrication

Few-layer MoS_2, h-BN, and graphite flakes were obtained via mechanical exfoliation and sequentially transferred onto a silicon substrate with a 285 nm thick SiO_2 layer using polydimethylsiloxane (PDMS). Electrode patterning was achieved by electron beam lithography (EBL) using a positive resist (PMMA A6). After exposure and development, 20/30 nm Ag/Au electrodes were deposited via electron beam evaporation. Finally, the device fabrication was completed after a standard lift-off process.

4.2 | Device Characterization

The AFM images and Raman spectroscopy were taken with a Bruker Dimension and a commercial Raman spectrometer with a 532 nm laser source. The photoelectric response of the optoelectronic synapse was characterized in the air by the Metatest E2 photoelectric testing system in the dark or under illumination with LEDs (255, 520, and 638 nm) from Nanjing Metatest Optoelectronics Co. Electrical characteristics were measured under ambient conditions using an Agilent B1500A semiconductor parameter analyzer and a B1525A (HV-SPGU) module.

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Conflicts of Interest

The authors declare no conflicts of interest.

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Supporting Information

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