ADVANCED FUNCTIONAL MATERIALS
www.afm-journal.de

Near-Perfect Standard Ternary Inverter Based on $MoTe_2$ Homojunction Anti-Ambipolar Transistor

Zhe Zhang, Shida Huo, Qijia Tian, Fanying Meng, Zheyu Yang, Yuexuan Ma, Yue Wang, Yuan Xie, Xiaodong Hu, Wenchao Gao, Enxiu Wu,* and Caofeng Pan**

Ternary inverters offer a promising solution to enhance information processing density and efficiency while reducing system complexity, addressing energy density limitations in complementary metal-oxide-semiconductor technology in the post-Moore era. Among these, the standard ternary inverter (STI) is particularly appealing due to its symmetry and reliability in ternary logic operations, though its fabrication remains challenging. Here, a controllable and process-compatible doping technique is reported that combines rapid thermal annealing with h-BN-assisted ultraviolet photoinduced doping to achieve area-selective p-type and n-type doping on a single $MoTe_2$ flake. This approach enables the fabrication of high-performance anti-ambipolar transistors (AATs) and unipolar p-type field-effect transistors (FETs) based on $MoTe_2$ homojunctions. By achieving near-perfect conductance matching between connected AATs and p-type FETs, an STI with a highly uniform staircase transfer characteristic and an intermediate state width of precisely one-third of the input voltage range is demonstrated. The AATs also exhibit a peak-to-valley ratio exceeding 10^3, rapid transconductance reversal, and tunable peak positions, enabling the development of high-performance frequency doublers without additional voltage bias. This study presents a novel doping strategy for efficient STI and multifunctional device fabrication, advancing the development of next-generation electronic technologies.

1. Introduction

With the explosive growth in data and information density, power density constraints have emerged as a significant bottleneck for further scaling of complementary metal-oxide-semiconductor (CMOS) technology.[1] Transitioning from binary to ternary system offers a promising solution to this power scaling challenge, significantly increasing information density while reducing system complexity by ≈63.1%.[2] The ternary inverter, as the fundamental building block of ternary systems, facilitates efficient computation, complex logic design, and low-power applications, making it a cornerstone of advanced electronic architectures.[3]

Ternary inverters are broadly classified into two primary types: the standard ternary inverter (STI) and non-standard ternary inverters, which include positive ternary inverter (PTI), negative ternary inverters (NTI), and decrement cycling inverters (DCI).[4] The STI is characterized by a symmetrical input-output relationship, where each input level is precisely inverted to its complementary level, ensuring balanced and consistent inversion across all three states. This inherent reliability and stability serve as a critical foundation for the design of efficient and high-performance multi-valued logic systems. In contrast, non-standard ternary inverters exhibit distinct bias characteristics, with output levels shifted positively, negatively, or cyclically, resulting in asymmetric or unique voltage transfer curves. This allows each type of non-standard

Z. Zhang, S. Huo, Q. Tian, F. Meng, Z. Yang, Y. Ma, Y. Wang, X. Hu, E. Wu
State Key Laboratory of Precision Measurement Technology and Instruments
School of Precision Instruments and Opto-electronics Engineering
Tianjin University
Tianjin 300072, P. R. China
E-mail: enxiuwu@tju.edu.cn

Y. Xie
School of Electronics and Information Engineering
Tiangong University
Tianjin 300387, P. R. China

W. Gao
Beijing Institute of Nanoenergy and Nanosystems
Chinese Academy of Sciences
Beijing 101400, P. R. China
E-mail: gaowenchao@binn.cas.cn

C. Pan
Institute of Atomic Manufacturing
Beihang University
Beijing 100191, P. R. China
E-mail: pancaofeng@buaa.edu.cn

C. Pan
International Research Institute for Multidisciplinary Science
Beihang University
Beijing 100191, P. R. China

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/adfm.202424728

DOI: 10.1002/adfm.202424728

inverter—PTI, NTI, and DCI—to exhibit specialized inversion behaviors optimized for specific applications.[5]

2D semiconductor materials present substantial advantages for high-speed, low-power logic computing chips in the post-Moore era, owing to their ultra-thin structure, high electron mobility, superior electrostatic control, compatibility with silicon-based processes, and excellent scalability for further miniaturization.[6] Additionally, the ability to stack diverse 2D semiconductor materials into van der Waals heterojunctions (vdWhs) without concerns for lattice matching facilitates the integration of distinct material properties, further enhancing device functionality and performance.[7] Specifically, vdWhs-based anti-ambipolar transistors (AATs), when paired with p-type transistors, represent the mainstream approach for constructing ternary inverters.[8]

To date, researchers have developed a range of vdWhs AAT-based ternary inverters, including BP/MoS_2,[9] MoS_2/WSe_2,[10] MoS_2/$MoTe_2$,[11] graphene/WSe_2[12] and $MoTe_2$/SnS_2,[13] BP/ReS_2.[14] However, these ternary inverters typically exhibit non-standard characteristics due to imperfect conductivity matching caused by the unclear voltage transition region and incomplete alignment of transfer characteristics between the AAT and p-type transistor components, despite efforts to modulate electrical transport properties through methods such as electric field,[15] plasma induced,[16] chemical treatment[17] and thickness modulation.[18]

2D homojunction formed by a single 2D material typically exhibits high-quality carrier diffusion channels and continuous band bending, providing an ideal platform for constructing STIs composed of AATs and p-type transistors with perfectly matched conductance.[19] However, compatible and precise doping approaches are required to achieve area-selective p-type and n-type doping. Recent studies have explored the development of ternary inverters using p-n homojunction AATs through a chemical doping approach,[20] work function modulation[21] and photosensitive modulation.[22] Despite these advancements, challenges remain in optimizing the doping process and further enhancing the performance of STIs.

In this work, we developed a near-perfect STI based on $MoTe_2$ homojunction AAT, achieved for the first time using a controllable and process-compatible doping technique that combines rapid thermal annealing (RTA) with h-BN-assisted ultraviolet (UV) photodoping approach. This method enables area-selective p-type and n-type unipolar doping, allowing for the simultaneous construction of a homojunction AAT with significant and tunable anti-ambipolar transfer behavior and a unipolar p-type transistor on a single $MoTe_2$ flake. The fabricated AAT exhibits a high peak-to-valley ratio (PVR) exceeding 10^3 and a broad operational voltage window ΔV_{gs} approaching 60 V. By connecting these two devices in series, we successfully fabricated a nearly ideal STI with equal height stair-case transfer characteristic, where the intermediate state voltage width (25 V) accounts for approximately one-third of the total input voltage. Additionally, the device demonstrated potential for applications in frequency doublers, highlighting its versatility for next-generation multifunctional electronics.

2. Results and Discussion

Figure 1a presents a schematic of the multilayer structure of the $MoTe_2$-based devices used in this study, where the $MoTe_2$ flake partially overlaps with the h-BN layer on the SiO_2/Si substrate. Subsequently, two pairs of Cr/Au electrodes were deposited onto the same $MoTe_2$ surface, defining two independent transport channels, labeled as 1–2 and 3–4. This configuration leads to the formation of a $MoTe_2$-based standard field-effect transistor (FET) (left half section) and a $MoTe_2$/h-BN heterojunction FET (right half section), both of which can be gate-controlled through the SiO_2/Si gate. Simultaneously, a $MoTe_2$ junction device is formed between electrodes 2 and 3. These devices are designed as Device A, Device B, and Device C, corresponding to the red, blue, and orange dashed rectangles in the false-color scanning electron microscopy (SEM) image (Figure 1b). To further characterize the thickness and material composition of the devices, atomic force microscopy (AFM) characterization, and Raman spectroscopy were performed on junction region B. As shown in Figure 1c, the thicknesses of the $MoTe_2$ and h-BN layers are measured to be 30.4 and 30.3 nm, respectively. The Raman spectra (Figure S1, Supporting Information) confirm the characteristic peaks of $MoTe_2$ and h-BN, aligning well with those reported in previous studies.[23]

Figure 1d shows the transfer characteristic curves of Device A (red), Device B (blue), and Device C (orange) in semi-log scales. The drain-source bias (V_{ds}) was fixed at 2 V, while the gate-source bias (V_{gs}) was linearly swept from −60 to 60 V. All three devices exhibit n-type dominated ambipolar transport behavior. Notably, the on-state current of Device C (with h-BN interlayer) is more than an order of magnitude higher than that of Device A. This improvement is attributed to the cleaner interface between h-BN and $MoTe_2$, compared to $MoTe_2$/SiO_2 interface, which effectively suppresses defect scattering and charge trapping, thereby enhancing carrier transport.[24] For Device B, the expected anti-ambipolar transfer behavior is not observed, primarily due to inadequate conductance matching between the devices on either side of the junction. Specifically, the formation of an AAT requires two conditions to be met. First, the carrier concentrations on the p-type and n-type sides of the junction must be balanced. Second, the threshold voltages of both sides must be sufficiently large to ensure that both devices can operate over a wide gate voltage range.[8,25] Therefore, these requirements highlight the necessity of area-selective and precise p-type and n-type doping on both sides of the junction.

To successfully realize the construction of an AAT, we first introduced RTA treatment on the sample for p-type doping of all $MoTe_2$-based devices. During the RTA process, both Device A and Device C underwent p-type doping, with the doping concentration closely dependent on the annealing temperature. The schematic diagram of the p-type doping process is shown in Figure S2 (Supporting Information). The annealing-induced anti-site defects (Mo_{Te}) act as acceptor dopants, generating a substantial number of holes, thereby significantly enhancing the p-type doping level of the devices.[26] Subsequently, n-type UV photodoping was introduced to Device C (with h-BN interlayer). The mechanism underlying n-type UV photodoping is

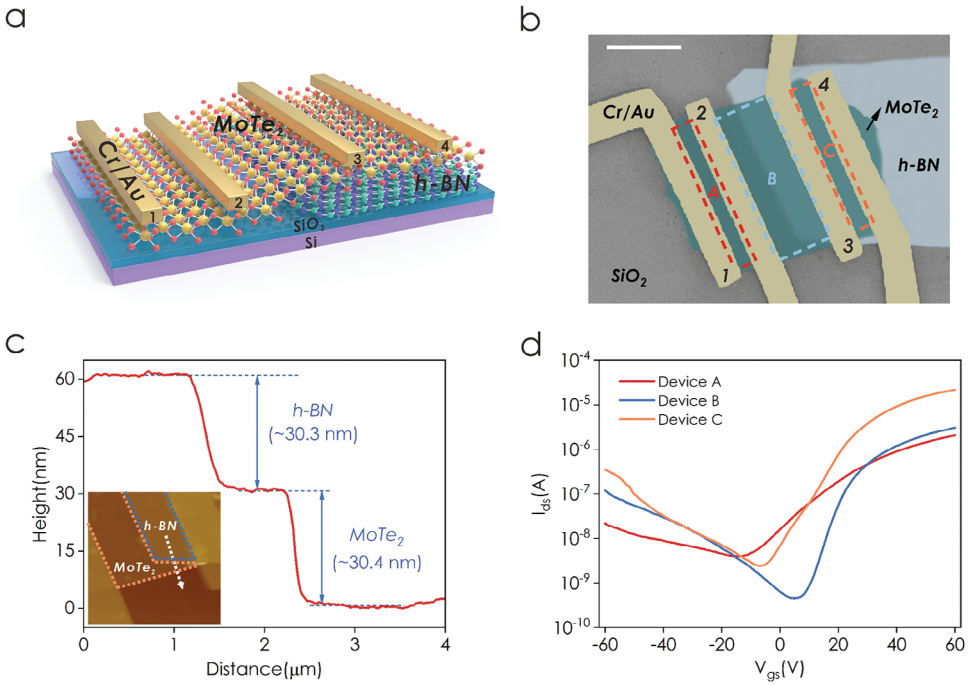

Figure 1. a) Schematic of the $MoTe_2$-based devices on the SiO_2/Si substrate. b) False-colored SEM image of the $MoTe_2$ FET (Device A), junction device (Device B) and $MoTe_2$/h-BN heterojunction FET (Device C) on the SiO_2/Si substrate. Scale bar is 10 μm. c) The AFM characterization of height profile and layer thickness at the $MoTe_2$/h-BN junction region (region B). d) Transfer characteristic curves of Device A, Device B, and Device C in semi-log scales. The $V_{ds} = 2$ V.

depicted in Figure S3 (Supporting Information). Under UV illumination, the $MoTe_2$ channel would absorb incident photons to generate a large number of photoexcited electron-hole pairs. Simultaneously, the UV light also excites defect states within the h-BN flake and at the h-BN/SiO_2 interface. By applying a negative writing voltage on the Si/SiO_2 substrate in the vertical direction, the photoexcited holes in the $MoTe_2$ channel are driven to tunnel across the h-BN and then are captured and trapped by these defect states, which create positive gating and electron doping in the intrinsic $MoTe_2$ channel. Higher writing voltage results in a larger tunneling current and higher hole density trapped at the h-BN flake and the h-BN/SiO_2 interface, thus inducing a deeper electron doping level.[23b] Notably, the stronger doping capability of n-type doping compared to p-type doping, combined with its selective activation in the presence of the h-BN interlayer, enables Device C to be reversely doped from p-type to n-type without inducing any significant impact on Device A. Hence, this method enables area-selective, process compatibility, and precisely controllable p-type and n-type doping concentrations, as illustrated in **Figure 2**.

Figure 2a presents the transfer characteristic curves of Device A after RTA treatment at different temperatures. The sample was treated in H_2/N_2 (2%/98%) mixture gas for 3 min. As the RTA temperature increases from 373 to 673 K, the transfer curve gradually shifts to the right, with the minimum conduction point (MCP) moving by ≈50 V, demonstrating significant p-type unipolar doping. Figure 2b illustrates the hole concentration and field-effect hole mobility of Device A after RTA treatment at different temperatures. The hole concentration of the pristine device (without annealing) is $\approx 1.78 \times 10^{12}$ cm^{-2}, increasing to 6.19×10^{12} cm^{-2} after annealing at 673 K. The hole mobility increases from 0.0009 cm^2 s^{-1} V^{-1} (pristine device) to 2.79 cm^2 s^{-1} V^{-1} (after 673 K annealing), representing a significant enhancement of over three orders of magnitude. This improvement originates from the formation of anti-site defects (Mo_{Te}) at the Au-$MoTe_2$ interface, as illustrated and explained in Figures S2 and S4 (Supporting Information). These defects act as acceptor-type dopants, generating a large number of holes while simultaneously lowering the Schottky barrier height for hole injection.[26]

Subsequently, UV photoinduced doping was employed to achieve efficient and area-selective n-type doping on Device C. We first exposed Device C to UV light (wavelength 254 nm, intensity 2.5 mW cm^{-2}) under a constant negative gate bias (referred to as "writing voltage" in the following discussion) for 1 s. Following this, both the UV illumination and the writing voltage were turned off, and a full linear scan was performed at a fixed V_{ds} of 2 V. It is critical that both UV light and the writing voltage are applied simultaneously during the photoinduced doping process to ensure stable and nonvolatile doping results. The absence of either of these two activations results in the failure of permanent change of electrical properties.[23b] Figure 2c presents the transfer characteristic curves of Device C after UV photoinduced doping under different writing voltages. Notably, when the writing voltage is 0 V, n-type doping is ineffective while p-type doping remains effective, thereby causing Device C to exhibit the same p-type behavior as Device A (red curve). Upon applying a negative writing voltage of −10 V, Device C immediately transitions from a heavily doped p-type unipolar transistor to an n-type dominated bipolar transistor (orange curve), highlighting

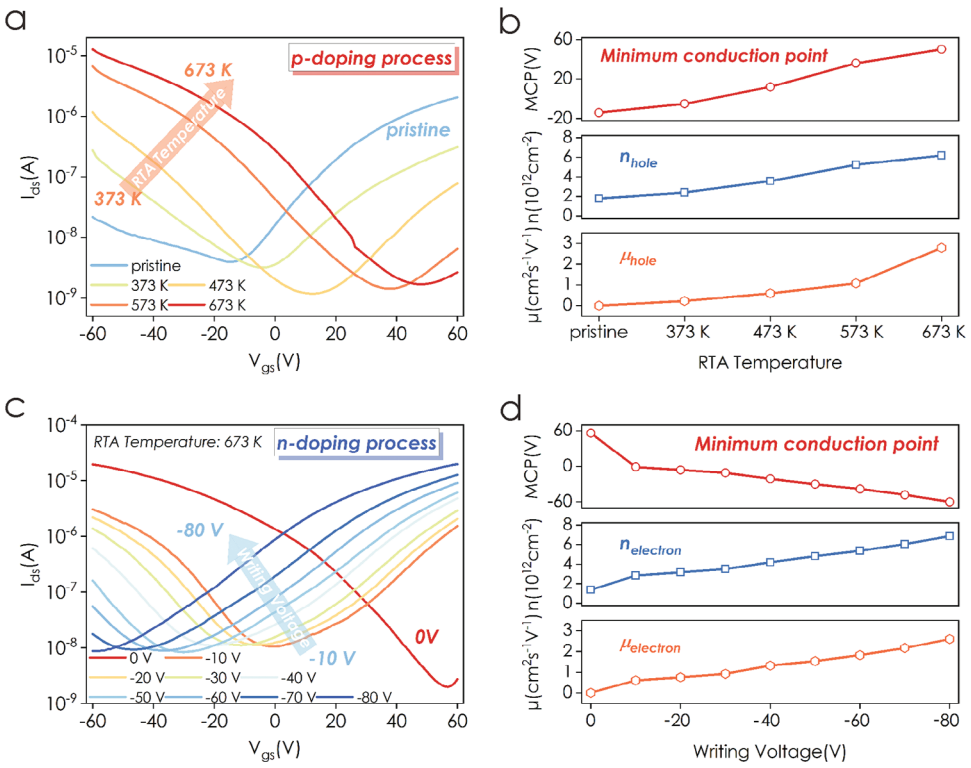

Figure 2. a) Transfer characteristic curves of Device A after rapid thermal annealing (RTA) at different temperatures in semi-log scales. b) The changes of minimum conduction point (MCP), hole concentration (n_{hole}), and field-effect hole mobility (μ_{hole}) of Device A after p-doping process (RTA). c) Transfer characteristic curves of Device C after UV photodoping at different writing voltages in semi-log scales. d) The changes of minimum conduction point (MCP), electron concentration ($n_{electron}$) and field-effect electron mobility ($\mu_{electron}$) of Device C after the n-doping process (UV photodoping).

the stronger doping effect of UV photodoping compared to RTA treatment. As the writing voltage increases from −10 to −80 V, Device C evolves from an n-type dominated ambipolar transistor to a heavily doped n-type unipolar transistor, with its MCP shifting progressively from 0 to −60 V in the negative direction (deep blue curve). The electron concentration ($n_{electron}$) and field effect electron mobility ($\mu_{electron}$) as a function of writing voltages are also plotted in Figure 2d. After UV photoinduced n-doping at a writing voltage of −80 V, the electron concentration increases from 1.375×10^{12} to 6.875×10^{12} cm^{-2} and the field-effect electron mobility demonstrates a strong enhancement from 0.001 to 2.3 cm^2 s^{-1} V^{-1}. This demonstrates that higher writing voltage promote the formation of a greater concentration of trapped positive charges within the h-BN flake and at the h-BN/SiO_2 interface, subsequently inducing more stable electron doping and higher electron concentrations.[23b] The enhancement in electron mobility is primarily attributed to the reduced Schottky barrier width between $MoTe_2$ and metal electrodes after UV photodoping.[29] Figure S4 (Supporting Information) displays the output characteristic curves of Device C after UV photodoping at a writing voltage of −80 V, exhibiting a near-ohmic contact behavior.

Figure 3a presents the transfer characteristic curves of Device B after UV photodoping at different writing voltages. At a writing voltage of 0 V, the device exhibits p-type dominated bipolar transport behavior. As the writing voltage increases from −10 to −20 V, the transport curve begins to display a distinct inverted "Λ" peak, indicating the emergence of anti-ambipolar transport characteristics.[8,30] With further increases in the writing voltage from −30 to −80 V, the transfer curve shifts progressively in the negative direction, accompanied by a significant rise in both the position and height of the I_{ds} peak. In fact, both of these changes are directly linked to the enhanced n-doping level in Device C, as shown in Figure 2c. Specifically, the carrier concentration and mobility of Device C approach comparable levels to those of Device A as its increasing n-type doping level, as evidenced by Figure 2b,d. Furthermore, after UV photodoping at a writing voltage of −80 V, the on-state voltage of Device C shifts to −60 V, resulting in an on-state voltage window exceeding 110 V when paired with Device A (Figure S5, Supporting Information). At this point, both Device C and Device A exhibit comparable doping levels and a sufficiently large overlapping voltage region between their two on-states, which satisfies the critical conditions required for the construction of AATs.[25]

For AATs, the I_{ds} peak position (V_{peak}), on-state bias range (ΔV_{gs}) and PVR are critical parameters for evaluating device performance.[8] V_{peak} is defined as the operating voltage of AAT and should be minimized to achieve lower power consumption, higher resolution of intermediate state in the ternary inverters, and reduced bias voltage for applications such as frequency doubling. The difference between the on-state voltage (V_{ON}) and off-state (V_{OFF}) voltage is defined as ΔV_{gs}, with a broader ΔV_{gs} being crucial to ensure reliable operation under diverse biasing conditions. And PVR represents the ratio of maximum (I_{peak}) to minimum (I_{valley}) drain currents. The V_{peak}, ΔV_{gs} and PVR were

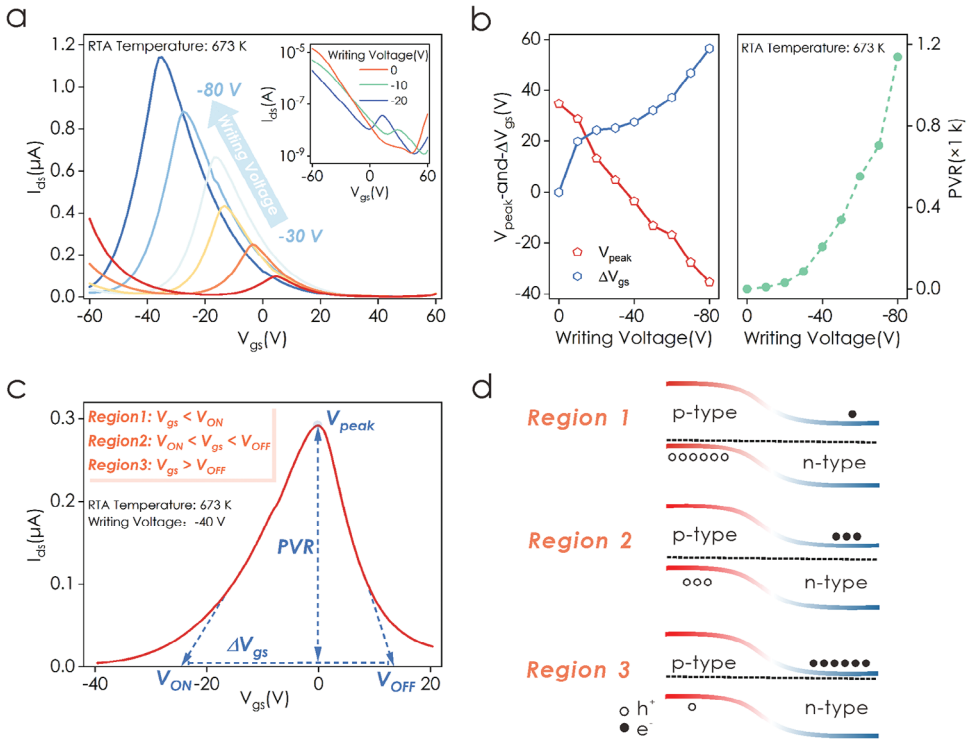

Figure 3. a) Transfer characteristic curves of Device B after UV photodoping at different writing voltages in linear (−30 to −80 V) and semi-log (0 to −20 V) scales. b) The changes of V_{peak}, ΔV_{gs}, and PVR of Device B after UV photodoping at different writing voltages. c) The transfer characteristic curve of Device B after UV photodoping at the writing voltage of −40 V. d) The schematic of typical transfer mechanism based on p-n homojunction AAT.

extracted from the transfer curves and plotted as a function of writing voltages in Figure 3b. Notably, at a writing voltage of −40 V, the V_{peak} of AAT is close to 0 V, representing an exceptionally low peak position compared to other reported 2D-based AATs. As the writing voltage increases from −40 to −80 V, V_{peak} shifts left to ≈−40 V. The near-linear relationship between V_{peak} and the writing voltage (red line) highlights the precise tunability of the I_{ds} peak in Device B through UV photodoping. In terms of ΔV_{gs}, it increases to ≈60 V after UV photodoping at a writing voltage of −80 V. Additionally, the PVR of Device B reaches a remarkable value of 10^3 after photodoping at −80 V, representing an enhancement of nearly two orders of magnitude compared to its value at −10 V. This exponential growth in PVR demonstrates a strong correlation with the writing voltage.

To clarify the operating mechanism of the homojunction AAT, the transfer curve of Device B after photodoping at a writing voltage of −40 V was extracted from Figure 3a and is presented in Figure 3c. As V_{gs} increase from −40 to 20 V, the I_{ds} of Device B initially increases and then decreases. V_{ON} and V_{OFF} denote the on-state and off-state voltages of the AAT, respectively. The transfer curve can be divided into three voltage regions: region 1 ($V_{gs} < V_{ON}$), region 2 ($V_{ON} < V_{gs} < V_{OFF}$), and region 3 ($V_{gs} > V_{OFF}$). In region 1 and region 3, the transfer curve exhibits similar minimum current levels, while showing an "Λ" shape in region 2. The operating principles of the homojunction AAT are schematically illustrated in three simplified energy band diagrams for different gate voltage regions, as shown in Figure 3d. The p-n homojunction can be regarded as a series connection of p-type and n-type FET, with each band diagram representing a different mode of carrier injection.[8,31] Indeed, it is the carrier concentration in the semiconductor channel, regulated by the gate voltage, that predominantly governs the anti-ambipolar transport behavior. According to the transfer characteristics of these transistors, as the gate voltage increases, the carrier concentration (hole) of the p-type FET decreases, while the carrier concentration (electron) of the n-type FET increases. Hence, the conductive mechanism of the AAT can be briefly described as follows. In voltage region 1, the p-type FET is in the on-state while the n-type is off, resulting in the total current being suppressed to its minimum value. As V_{gs} increases into voltage region 2, the current level flows to its maximum value because both transistors are in the on-state. In voltage region 3, I_{ds} is suppressed again as the p-type FET switches off, even though the n-type FET remains in the on-state.

The series connection of an AAT and a p-type FET represents the prevailing approach for constructing ternary inverters. **Figure** 4a illustrates the configuration and testing circuit schematic of the ternary inverter. One terminal of the p-type FET serves as the supply voltage (V_{DD}), the shared terminal with the AAT functions as the output voltage (V_{OUT}), and the other terminal of the AAT is grounded (GND). The input voltage (V_{IN}) was applied to the common Si back gate. To realize a STI, the AAT must achieve optimal conductance matching with the p-type FET.[14] For this purpose, we intentionally selected the photodoped AAT at a writing voltage of −40 V to be connected in series with Device A. The transport characteristics of both devices are shown in Figure 4b, which exhibits nearly identical conductance in the range of −5 to 20 V. Figure 4c presents the Voltage-transfer characteristic (VTC) curve of the constructed ternary

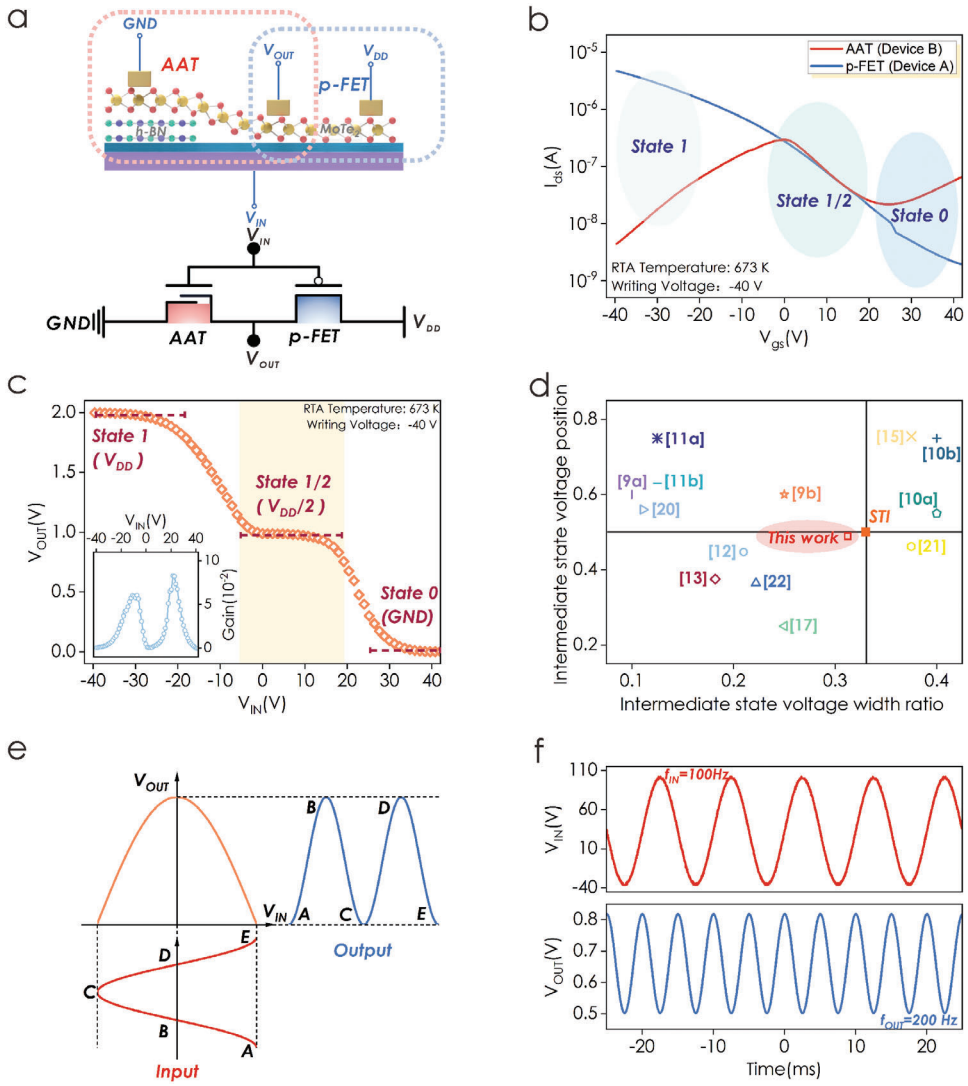

Figure 4. a) The schematic diagram of the ternary inverter formed by the series connection of $MoTe_2$ p-type FET (Device A) and $MoTe_2$ homojunction AAT (Device B). b) Transfer characteristic curves of the $MoTe_2$ p-type FET (blue curve) and $MoTe_2$ homojunction AAT (red curve). c) The Voltage-transfer characteristic and voltage gain (inset) of the ternary inverter at V_{DD} = 2 V. d) The intermediate voltage position and intermediate voltage width ratio of the ternary inverter for various reported 2D AAT-based devices. e) Working principle of AAT-based frequency doubler f) The input-output voltage waveforms measured by the frequency doubler.

inverter under a driving voltage of V_{DD} = 2 V, clearly demonstrating three distinct logical states with equal height stair-case characteristics.

In fact, the ternary inverter essentially functions as a voltage divider for V_{DD}. When V_{IN} < −20 V, the p-type FET is in a low-resistance state and the AAT is in a high-resistance state, resulting in V_{OUT} being approximately equal to V_{DD} (2 V), denoted as logic State 1 in Figure 4c. The stable logic State 1/2 arises from the precise conductivity matching between the AAT and the p-type FET in this voltage range, ensuring that the V_{OUT} is maintained exactly at one-half of the V_{DD}. The width of the intermediate logic state is 25 V, approximately one-third of the total input voltage range, indicating a broad tolerance window and high stability for this middle logic state. In the positively high V_{IN} region (V_{IN} > 25 V), the AAT remains in a low-resistance state, while the p-type FET gradually transitions to a high-resistance state, yielding a low output voltage, denoted as logic State 0. The voltage gain, calculated as Gain = dV_{OUT}/dV_{IN}, is shown in the inset of Figure 4c. The gain curve exhibits two pronounced peaks, reaching a value of 0.085 when V_{IN} is ≈20 V. The relatively small voltage gain is likely due to the slow switching speed caused by the thick SiO_2 dielectric layer.[32] By using thinner SiO_2 dielectrics or thin high-k dielectric substrates, the voltage gain and switching speed of the constructed ternary inverter will be significantly enhanced in future work.[33]

To precisely categorize the type of ternary inverter and quantitatively characterize the STI characteristic, we define two key parameters: the intermediate state voltage position (V_{mid}) and the intermediate state voltage width ratio (W_{mid}). Specifically, the

V_{mid} quantifies the proportion of the intermediate state voltage relative to the total output voltage range (V_{OUT}), and the W_{mid} represents the fraction of the intermediate state voltage width with respect to the total input voltage range (V_{IN}). For the STI, the intermediate state voltage position should ideally be centered at half of the output voltage ($V_{mid} = 1/2$), and the intermediate state voltage width should encompass one-third of the input voltage range ($W_{mid} = 1/3$), ensuring rapid logical transitions and enhanced noise immunity, as highlighted by the solid orange rectangle in Figure 4d. From the voltage transfer curve of Figure 4c, it is calculated that the constructed ternary inverter achieves an intermediate state voltage position of 1/2 and an intermediate state voltage width ratio approaching 1/3. This demonstrates that, compared to previous studies (Figure 4d), we have achieved an almost ideal STI through the precise conductance matching of the series-connected AAT and p-type FET.

A key feature of AATs is their ability to present both positive and negative transconductances, which can be effectively utilized for fundamental analog circuit functions, such as frequency doubling.[34] Using the same device configuration and peripheral circuitry presented in Figure 4a, we designed and constructed a frequency doubler, where the p-type FET can be regarded as a constant resistance. The output signal is detected by an oscilloscope connected to the AAT (Device B). By applying a sinusoidal signal with a frequency of f_{IN} to the gate bias, for which the device is at the peak value of its transfer curve, the drain current will display a signal with a frequency twice that of the input. Specifically, as the input signal V_{IN} (red curve) oscillates from point A to point B, the output signal V_{OUT} (blue curve) increases with the rising input. When the input signal swings from point B to point C, the output signal decreases with the increasing input. Similarly, the output signal from point C to point E through point B will be exactly the same as that of point A to point C. In fact, thanks to the symmetrical transfer curve, each half-cycle oscillation of the input signal corresponds to a full-cycle oscillation of the output signal, as shown in Figure 4e. When the writing voltage of n-doping is −40 V, as depicted in Figure 3c, the I_{ds} peak of the AAT device is located at $V_{gs} = 0$ V, ensuring that perfect frequency doubling can be achieved without any additional gate voltage bias. The measurement conditions are that the source voltage V_{DD} = 5 V. Figure 4f presents that at an input signal V_{IN} (red curve) with frequency $f_{IN} = 100$ Hz, the output waveform is a sinusoidal signal V_{OUT} (blue curve) with frequency $f_{OUT} = 200$ Hz, thus clearly demonstrating the frequency doubling effect. Refinements such as scaling down device dimensions and local gating are likely to further enhance the AAT-based frequency doubler performance. Compared to CMOS-based analog architectures, AAT-based frequency doublers provide significant advantages by substantially reducing the number of required transistors and eliminating the necessity for bias voltage to achieve device matching.

3. Conclusion

In summary, our study successfully developed a new method that combines RTA with h-BN-assisted UV photoinduced doping to selectively dope p-type and n-type regions on a single 2D $MoTe_2$ flake. This advancement allowed us to fabricate high-performance devices, including an AAT and a unipolar p-type FET, both based on $MoTe_2$ homojunction. By achieving nearly perfect conductance matching between the two devices, we successfully constructed a near-ideal standard ternary inverter. Furthermore, the developed AAT shows a PVR exceeding 10^3, rapid transconductance reversal, and a precisely tunable I_{ds} peak position. These features enable the design of high-performance frequency doublers. These findings demonstrate the effectiveness of our approach and its potential to significantly advance electronic and optoelectronic device performance.

4. Experimental Section

Device Fabrication: The devices were produced with a dry transfer technique. $MoTe_2$ and h-BN were purchased from HQ graphene. First, an h-BN flake was mechanically exfoliated from bulk h-BN and transferred onto a 285 nm SiO_2/n+-doped Si substrate. Then, a $MoTe_2$ flake was transferred onto an h-BN flake, covering half of it. Last, electrodes were patterned using electron beam lithography with positive electron beam resist. Cr/Au (20/30 nm) was deposited by electron beam evaporation after exposure and development, which was followed by a standard lift-off process to complete the fabrication. The device was treated by a rapid thermal annealing (RTA) process in an H_2/N_2 mixed gas (2% H_2, 98% N_2) under different temperatures ranging from 373 to 673 K for 3 min. The UV photoinduced doping is done by applying a large gate bias voltage and UV illumination (wavelength 254 nm, intensity 2.5 mW cm^{-2}) on the device at the same time, for typically less than 1s.

Electrical Parameters Calculation: The electron concentration ($n_{electron}$) and hole concentration (n_{hole}) of the $MoTe_2$ film can be calculated according to $n = -C_g/(V_{gs}-V_{th})$ at V_{gs} = 40 V and V_{gs} = -40 V, where $C_g = 1.1 \times 10^{-8}$ F cm^{-2} denotes the gate oxide capacitance for 285 nm SiO_2 and V_{th} is the threshold voltage for electron/hole transport. The field effect mobility, which can be calculated using $\mu = G_m L/(C_g V_{ds} W)$, where $G_m = dI_{ds}/dV_{gs}$ is the transconductance and can be extracted from the linear region of the transfer curve, L and W are the channel length and width, respectively.

Characterizations: A commercial Raman spectrometer (Renishaw Inc.) was used to obtain the Raman spectroscopy with a 532-nm laser source. The AFM images were taken with a Bruker Dimension Icon. The electrical properties were measured with an Agilent B1500A semiconductor parameter analyzer in ambient air. The wavelength and intensity of the used UV light were 254 nm and 2.5 mW cm^{-2}, respectively.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

This study was supported by the open research of Songshan Lake Materials Laboratory (2023SLABFK07), the China Postdoctoral Science Foundation (2023M742585), the National Science Foundation of China (62304151, 62204170, 62474124, 52203307, and 52125205), the State Key Laboratory of Fluid Power and Mechatronic Systems (GZKF-202327), the State Key Laboratory of Mechanics and Control for Aerospace Structures (the Nanjing University of Aeronautics and astronautics) (MCMS-E-0123Y01), and the Open Project of State Key Laboratory of Transducer Technology (Grant No. SKT2208).

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

anti-ambipolar transistor, frequency doublers, $MoTe_2$ homojunction, photoinduced doping, ternary inverter

Received: December 15, 2024
Revised: February 2, 2025
Published online:

[1] a) G. E. Moore, *Proc. IEEE* **1998**, *86*, 82; b) P. S. Peercy, *Nature* **2000**, *406*, 1023.
[2] a) H. Hurst, *IEEE Transact. Comp.* **1984**, *C-33*, 1160; b) J. W. Jeong, Y. E. Choi, W. S. Kim, J. H. Park, S. Kim, S. Shin, K. Lee, J. Chang, S. J. Kim, K. R. Kim, *Nat. Electron.* **2019**, *2*, 307.
[3] a) C. Lee, C. Lee, S. Lee, J. Choi, H. Yoo, S. G. Im, *Nat. Commun.* **2023**, *14*, 3757; b) M. Andreev, S. Seo, K. S. Jung, J. H. Park, *Adv. Mater.* **2022**, *34*, 2108830.
[4] M. Q. Huang, X. L. Wang, G. C. Zhao, P. Coquet, B. K. Tay, *Appl. Sci.-Basel* **2019**, *9*, 4212.
[5] a) S. Shin, E. Jang, J. W. Jeong, K. R. Kim, *IEEE Silicon Nanoelectronics Workshop (SNW)*, IEEE, Honolulu, HI, **2016**; b) S. Shin, E. Jang, J. W. Jeong, B. G. Park, K. R. Kim, *IEEE Trans. Electron Devices* **2015**, *62*, 2396.
[6] a) A. H. Liu, X. W. Zhang, Z. Y. Liu, Y. N. Li, X. Y. Peng, X. Li, Y. Qin, C. Hu, Y. Q. Qiu, H. Jiang, Y. Wang, Y. F. Li, J. Tang, J. Liu, H. Guo, T. Deng, S. A. Peng, H. Tian, T. L. Ren, *Nano-Micro Lett.* **2024**, *16*, 119; b) S. Y. Wang, X. X. Liu, P. Zhou, *Adv. Mater.* **2022**, *34*, 2106886; c) Y. C. Lin, R. Torsi, R. Younas, C. L. Hinkle, A. F. Rigosi, H. M. Hill, K. Y. Zhang, S. X. Huang, C. E. Shuck, C. Chen, Y. H. Lin, D. Maldonado-Lopez, J. L. Mendoza-Cortes, J. Ferrier, S. Kar, N. Nayir, S. Rajabpour, A. C. T. van Duin, X. W. Liu, D. Jariwala, J. Jiang, J. Shi, W. Mortelmans, R. Jaramillo, J. M. J. Lopes, R. Engel-Herbert, A. Trofe, T. Ignatova, S. H. Lee, Z. Q. Mao, *ACS Nano* **2023**, *17*, 9694; d) X. D. Wang, H. L. Zhang, L. Dong, X. Han, W. M. Du, J. Y. Zhai, C. F. Pan, Z. L. Wang, *Adv. Mater.* **2016**, *28*, 2896.
[7] a) K. S. Novoselov, A. Mishchenko, A. Carvalho, A. H. C. Neto, *Science* **2016**, *353*, aac9439; b) D. Jariwala, T. J. Marks, M. C. Hersam, *Nat. Mater.* **2017**, *16*, 170; c) S. J. Liang, B. Cheng, X. Y. Cui, F. Miao, *Adv. Mater.* **2020**, *32*, 1903800; d) M. Qi, R. Yang, Z. Wang, Y. Liu, Q. Zhang, B. He, K. Li, Q. Yang, L. Wei, C. F. Pan, M. Chen, *Adv. Funct. Mater.* **2023**, *33*, 2214479; e) R. Q. Zhu, Z. Y. Li, G. D., Y. H. Yu, J. L. Shui, R. H. Yu, C. F. Pan, X. F. Liu, *Nano Energy* **2022**, *92*, 106700.
[8] Y. Meng, W. J. Wang, W. Wang, B. W. Li, Y. X. Zhang, J. Ho, *Adv. Mater.* **2024**, *36*, 2306290.
[9] a) X. X. Jiang, M. Zhang, L. W. Liu, X. Y. Shi, Y. F. Yang, K. Zhang, H. Zhu, L. Chen, X. K. Liu, Q. Q. Sun, D. W. Zhang, *Nanophotonics* **2020**, *9*, 2487; b) M. Q. Huang, S. M. Li, Z. F. Zhang, X. Xiong, X. F. Li, Y. Q. Wu, *Nat. Nanotechnol.* **2017**, *12*, 1148.
[10] a) A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, T. Palacios, *Nano Lett.* **2016**, *16*, 1359; b) Y. H. Lv, C. Y. Wu, Y. Zhao, G. Wu, M. Abid, J. Cho, M. Choi, C. O. Coileáin, K. M. Hung, C. R. Chang, Y. R. Wu, H. C. Wu, *ACS Appl. Electron. Mater.* **2022**, *4*, 5487.
[11] a) N. T. Duong, J. Lee, S. Bang, C. Park, S. C. Lim, M. S. Jeong, *ACS Nano* **2019**, *13*, 4478; b) R. X. Hu, E. X. Wu, Y. Xie, J. Liu, *Appl. Phys. Lett.* **2019**, *115*, 073104.
[12] J. Shim, S. H. Jo, M. Kim, Y. J. Song, J. Kim, J. H. Park, *ACS Nano* **2017**, *11*, 6319.
[13] C. F. Chen, S. H. Yang, C. Y. Lin, M. P. Lee, M. Y. Tsai, F. S. Yang, Y. M. Chang, M. J. Li, K. C. Lee, K. Ueno, Y. M. Shi, C. H. Lien, W. W. Wu, P. W. Chiu, W. W. Li, S. T. Lo, Y. F. Lin, *Adv. Sci.* **2022**, *9*, 2106016.
[14] X. Xiong, J. Y. Kang, Q. L. Hu, C. R. Gu, T. T. Gao, X. F. Li, Y. Q. Wu, *Adv. Funct. Mater.* **2020**, *30*, 1909645.
[15] R. Q. Cheng, L. Yin, F. Wang, Z. X. Wang, J. J. Wang, Y. Wen, W. H. Huang, M. G. Sendeku, L. P. Feng, Y. F. Liu, J. He, *Adv. Mater.* **2019**, *31*, 1901144.
[16] S. Shahi, A. Ahmed, R. Z. Yang, A. Cabanillas, A. Chakravarty, M. M. Liu, H. N. Jaiswal, Y. Fu, Y. T. Guo, S. S. Jadeja, H. Murugesan, A. Butler, C. T. Chen, J. Muhigirwa, M. Enaitalla, J. Liu, F. Yao, H. M. Li, *J. Vac. Sci. Technol. B* **2023**, *41*, 053202.
[17] J. Y. Kim, H. J. Park, S. H. Lee, C. Seo, J. Kim, J. Joo, *ACS Appl. Mater. Interfaces* **2020**, *12*, 36530.
[18] J. C. Shin, Y. H. Kim, K. Watanabe, T. Taniguchi, C. H. Lee, G. H. Lee, *Adv. Mater. Interfaces* **2022**, *9*, 2101763.
[19] F. K. Wang, K. Pei, Y. Li, H. Q. Li, T. Y. Zhai, *Adv. Mater.* **2021**, *33*, 2005303.
[20] J. Kim, M. Jung, D. U. Lim, D. Rhee, S. H. Jung, H. K. Cho, H. K. Kim, J. H. Cho, J. Kang, *Nano Lett.* **2022**, *22*, 570.
[21] Y. Kim, S. Y. Kim, J. Noh, C. Shim, U. Jung, S. K. Lee, K. E. Chang, C. Cho, B. H. Lee, *Sci. Rep.* **2016**, *6*, 39353.
[22] J. B. Kim, J. S. Li, Y. Choi, D. Whang, E. Hwang, J. H. Cho, *ACS Appl. Mater. Interfaces* **2018**, *10*, 12897.
[23] a) C. G. Zhu, X. X. Sun, H. W. Liu, B. Y. Zheng, X. W. Wang, Y. Liu, M. Zubair, X. Wang, X. L. Zhu, D. Li, A. L. Pan, *ACS Nano* **2019**, *13*, 7216; b) E. X. Wu, Y. Xie, J. Zhang, H. Zhang, X. D. Hu, J. Liu, C. W. Zhou, D. H. Zhang, *Sci. Adv.* **2019**, *5*, eaav3430.
[24] a) S. D. Sarma, E. H. Hwang, *Phys. Rev. B* **2011**, *83*, 121405; b) S. M. Kim, A. Hsu, M. H. Park, S. H. Chae, S. J. Yun, J. S. Lee, D. H. Cho, W. J. Fang, C. Lee, T. Palacios, M. Dresselhaus, K. K. Kim, Y. H. Lee, J. Kong, *Nat. Commun.* **2015**, *6*, 8662.
[25] E. X. Wu, Y. Xie, Q. Z. Liu, X. D. Hu, J. Liu, D. H. Zhang, C. W. Zhou, *ACS Nano* **2019**, *13*, 5430.
[26] J. C. Chen, Z. H. Feng, S. Q. Fan, S. Shi, Y. C. Yue, W. F. Shen, Y. Xie, E. X. Wu, C. L. Sun, J. Liu, H. Zhang, W. Pang, D. Sun, W. Feng, Y. Y. Feng, S. Wu, D. H. Zhang, *ACS Appl. Mater. Interfaces* **2017**, *9*, 30107.
[27] a) L. Jun, J. Velasco, E. Huang, S. Kahn, C. Nosiglia, H. Z. Tsai, W. Yang, T. Taniguchi, K. Watanabe, Y. Zhang, G. Zhang, M. Crommie, A. Zettl, F. Wang, *Nat. Nanotechnol.* **2014**, *9*, 348; b) T. Liu, D. Xiang, Y. Zheng, Y. A. Wang, X. Y. Wang, L. Wang, J. He, L. Liu, W. Chen, *Adv. Mater.* **2018**, *30*, 1804470.
[28] S. Cho, S. Kim, J. H. Kim, J. Zhao, J. Seok, D. H. Keum, J. Baik, D. H. Choe, K. J. Chang, K. Suenaga, S. W. Kim, Y. H. Lee, H. Yang, *Science* **2015**, *349*, 625.
[29] a) H. Fang, M. Tosun, G. Seol, T. C. Chang, K. Takei, J. Guo, A. Javey, *Nano Lett.* **2013**, *13*, 1991; b) D. Kiriya, M. Tosun, P. D. Zhao, J. S. Kang, A. Javey, *J. Am. Chem. Soc.* **2014**, *136*, 7853.
[30] D. Jariwala, V. K. Sangwan, C. C. Wu, P. L. Prabhumirashi, M. L. Geier, T. J. Marks, L. J. Lauhon, M. C. Hersam, *Proc. Natl. Acad. Sci. USA* **2013**, *110*, 18076.
[31] a) K. Kobashi, R. Hayakawa, T. Chikyow, Y. Wakayama, *Adv. Electron. Mater.* **2017**, *3*, 1700106; b) H. C. Han, B. Q. Zhang, Z. H. Zhang, Y. M. Wang, C. Liu, A. K. Singh, A. M. Song, Y. X. Li, J. D. Jin, J. W. Zhang, *Nano Lett.* **2024**, *24*, 8602.
[32] a) A. I. Kingon, J. P. Maria, S. K. Streiffer, *Nature* **2000**, *406*, 1032; b) Y. D. Zhao, K. Xu, F. Pan, C. J. Zhou, F. C. Zhou, Y. Chai, *Adv. Funct. Mater.* **2017**, *27*, 1603484.
[33] J. Robertson, R. M. Wallace, *Mater. Sci. Engin.: R: Rep.* **2015**, *88*, 1.
[34] a) H. Yao, E. X. Wu, J. Liu, *Appl. Phys. Lett.* **2020**, *117*, 123103; b) D. Jariwala, V. K. Sangwan, J. W. T. Seo, W. C. Xu, J. Smith, C. H. Kim, L. J. Lauhon, T. J. Marks, M. C. Hersam, *Nano Lett.* **2015**, *15*, 416.